much higher maximum signal frequencies than the tube, or at low frequencies with less distortion. The sharp cutoff evident in Fig. 2 gives a much cleaner on-off action, particularly in switching applications.

In short, the Fetron can be considered a better pentode than the vacuum tube pentode, because its drain output curves come much closer to the theoretical ideal.

And two JFETs are better than one

It requires two JFETs in a hybrid package to simulate the performance of one pentode. The JFET must withstand high plate voltage (see Fig. 2) to replace the tube directly. But there is no single high-voltage JFET with enough transconductance g_m to match that of the pentode tube. For example, to simulate the 6AK5 a transconductance of 3,500 to 7,500 micromhos at an operating current of 4 to 10 milliamperes is required.

Moderate g_m at high voltage is expensive to get with JFETs, since they must be physically large and of high-resistance material to yield high breakdown voltages. Then, too, the major barrier to high-frequency performance in semiconductors is the Miller effect—the gate-to-source capacitance. In an amplifier, Miller $C_{gs} = C_{gd}(1 + A)$. This is minimized in pentodes because of the extremely low plate-grid capacitance that exists because the control grid is shielded by the highly positive voltage screen grid.

To get a high-transconductance, high-frequency (low-Miller-effect capacitance) JFET device, it's necessary to bootstrap or cascode two of them (Fig. 3). In such a design, the input transistor is a small-signal JFET, like the 2N3823, chosen for its low capacitance and high g_m; the output device is a high-voltage JFET, such as a 2N4882. The pair is assembled as chips and packaged in cans.

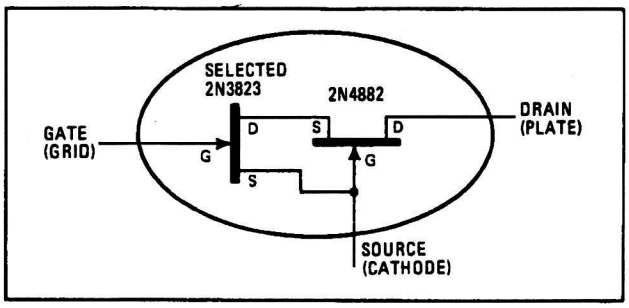
Smooth operator

The operation of the hybrid assembly is simple. The output JFET reduces the plate voltage to a safe level for the input JFET. The former JFET's drain is always connected to the high voltage—the equivalent plate connection in a Fetron—and its gate source connected to the input JFET's gate, which is tied to a low voltage or ground. With this arrangement the input capacitance of the device is just the fairly low capacitance of the input JFET, rather than the much higher capacitance associated with the large high-voltage chip.

With this arrangement assuring equal gains, the Miller-effect capacitance is equal to or lower than that of a tube pentode. The Fetron has only the 0.02-picofarad drain-to-source capacitance of the high-voltage JFET in series with the drain-to-gate capacitance of the unity-voltage-gain low-voltage input JFET. The result: less than 0.02-pF Miller-effect capacitance.

Also, the cascode arrangement boosts the effective output impedance of the Fetron about an order of magnitude above that of a pentode tube. This not only greatly improves the pentode curves, but makes the circuit gain less dependent on Fetron characteristics.

The device's input looks like a reverse-biased semiconductor junction, which provides a very high resistance that's desirable in most applications. Significantly, the effective input impedance is an order of magnitude above a vacuum tube's. This enables a circuit to operate from a high-resistance source without being loaded down.



3. Gaining with cascodes. Most Fetrons are built with two JFETs in a bootstrap or cascode connection to achieve high-gain operation. Miller-effect capacitance is minimized by using a low-capacitance, high-gain input transistor, such as the 2N3823, connected to a high-voltage 2N4882 output device.

Amplification equations

The tube equations apply when the Fetron is plugged into a typical tube biasing network, like the one shown in Fig. 4. (Heater and extra grid connections are left open on the Fetron.)

At any control grid voltage, the plate current will be

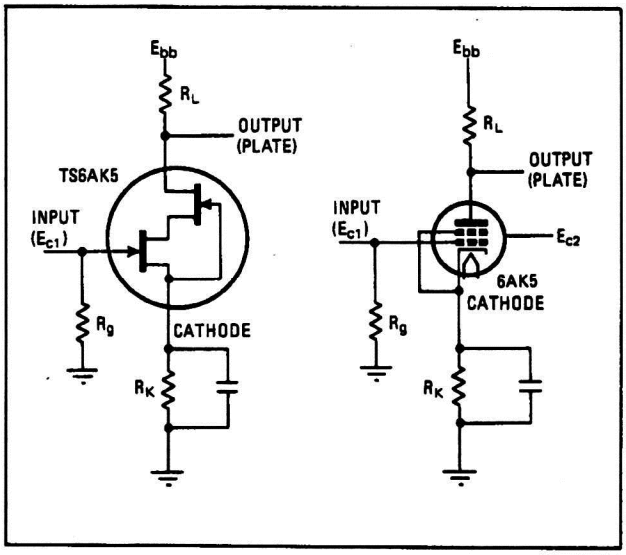
$$I_b = I_{b0}\left[1 - \frac{E_c}{E_{c(off)}}\right]^2$$

where

I_{b0} = plate current at $E_c = 0$ V
I_b = plate current at E_c voltage
E_c = control grid voltage
$E_{c(off)} = E_c$ for 1 μA of I_b

The change of plate current with grid voltage at a constant plate current gives the transconductance. By differentiating the equation for plate current with respect to control voltage:

$$g_m = \frac{\Delta I_b}{\Delta E_c}\Bigg|_{E_b = K} = g_{m0}\left[1 - \frac{E_c}{E_{c(off)}}\right]$$



4. Same old circuit. A Fetron (TS6AK5, for example) can directly replace a tube (6AK5, for example) in an unaltered circuit. The heater and extra grid connections are left open on the Fetron.