DIGITAL VOICE SYSTEMS, INC.

The Speech Compression Specialists

Data Subject to change
January 1997
Version 2.0

Single I.C. Vocoder
High Quality, Low Power, Voice Codec

Product Information — AMBE-1000™

General Information:

DVSI's AMBE-1000™ Voice Codec is an extremely flexible high-performance vocoder. The AMBE-1000™ provides superior voice quality at low data rates. It provides a real-time, full-duplex implementation of the standard-setting AMBE® speech compression system. DVSI's patented AMBE® technology has been proven to outperform CELP and other competitive technologies. Numerous evaluations have shown its ability to provide performance equal to today's digital cellular systems at under half the data rate. The AMBE® speech compression system is used in applications throughout the world, including the next generation of digital mobile communication systems.

The AMBE-1000™ provides a high degree of flexibility in selecting the speech and FEC data rates in 50 bps increments, from 2.4 kbps to 9.6 kbps.

Advantages:

- Superior Voice Quality
- Variable Data Rates - 2.4 kbps to 9.6 kbps
- Robust to Bit Errors & Background Noise
- Low Cost
- Very Low Power (65mW, 13mW standby)
- Compact Single I.C. Solution: 100 pin TQFP

Features:

- High Quality Low Data Rate Speech Coding
- DVSI Full Duplex AMBE® Voice Coder
- Supports Data Rates of 2.4 kbps to 9.6 kbps in 50 bps increments
- User Selectable Error Correction
- Dual Tone / DTMF
- Echo Cancellation
- Self-Test Loop-Back Mode
- Voice Activation/ Comfort Noise Insertion
- Power-Down Mode
- Selectable Serial or Parallel Channel Interface

Applications:

- Cellular Telephony and PCS
- Satellite Communications
- Digital Mobile Radio
- Secure Communications
- Voice Multiplexing
- Voice Mail
- Multimedia Applications
- Video Conferencing

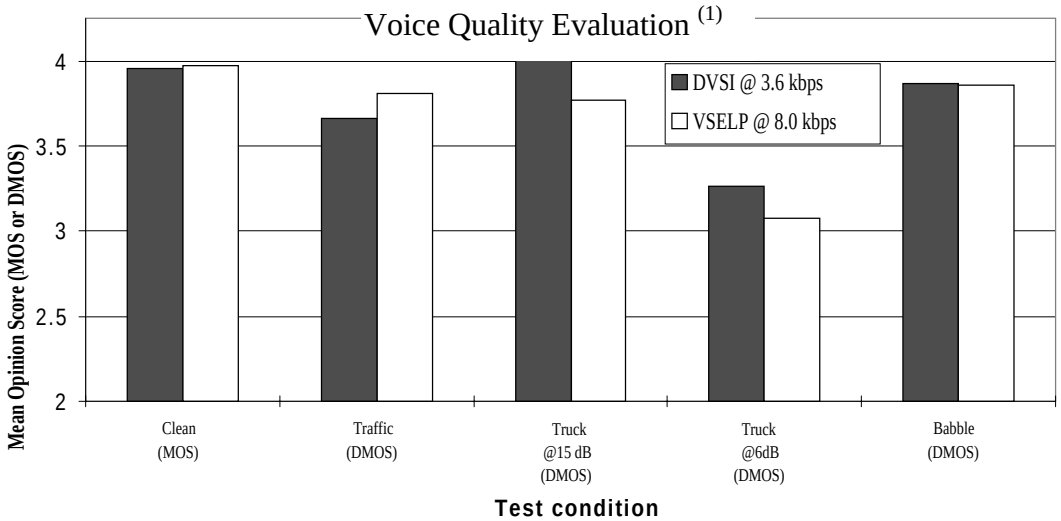


Table of Contents

Tables

Figures

1. Overview

Digitized speech is received from or sent to an external A/D-D/A through a serial interface. Digitized speech from the A-to-D on the external A/D-D/A chip is processed by the AMBE-1000™ encoder and converted into compressed digital data. This data is output to the channel interface which is connected to a processor, controller, modem or similar device. Simultaneously, the AMBE-1000™ receives compressed digital data from the channel interface. This received data is processed by the AMBE-1000™ decoder and reconstructed into a digital speech signal which is then converted into an analog signal using a D-to-A on an external A/D-D/A chip. The encoder and decoder are fully asynchronous.

1.1 Basic Operation

The channel interface can be configured into either parallel mode or serial mode. This document will also explain the different formats of frame data the AMBE-1000™ Vocoder can accept in serial and parallel modes. Figure 1.2-1 shows the basic concept of the AMBE-1000™ and its interfaces.

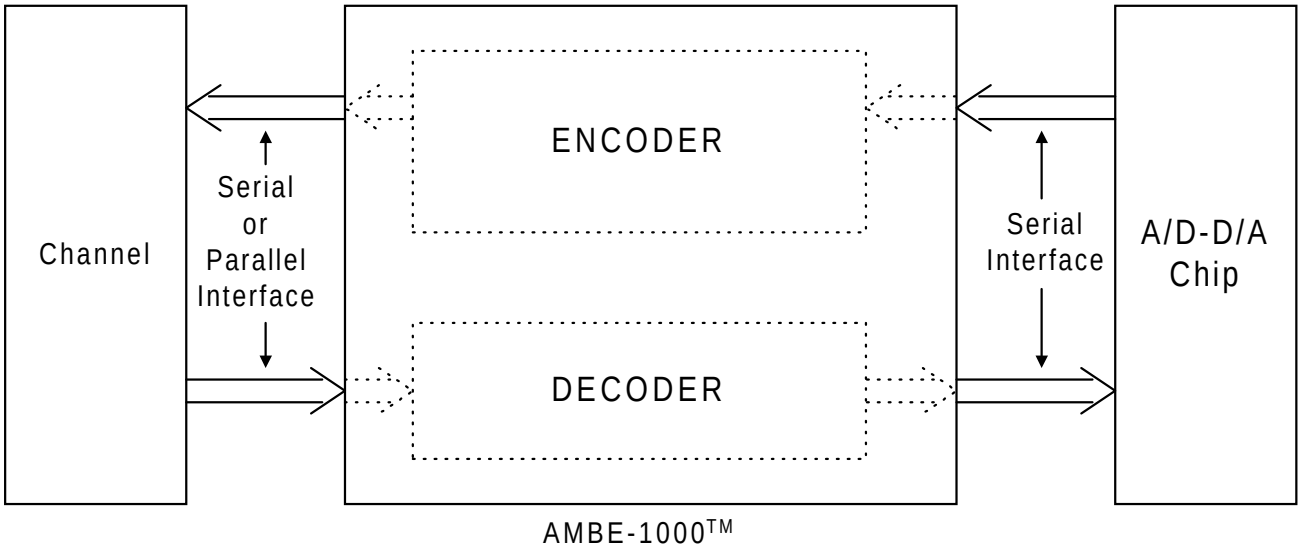


Figure 1.2-1 Overview of the AMBE-1000™ and its Interfaces

A/D-D/A data is always sent and received by a second serial port. Serial data that is to be encoded is received on RX_DI, while processed decoded data for the A/D-D/A is sent out on TX_DO.

The following pages contain information about how to configure the AMBE-1000™ vocoder.

1.2 References

(1) S. Dimoitsas, F. L. Corcoran, C Ravishankar, A. Wong, S. F. de Campos Neto and R.S. Skaland, "*Evaluation of voice codec performance for the INMARSAT MINI-M system,"* Tenth International Conference on Digital Satellite Communications, Vol. I, pp. 15-19, May 1995.

(2) *AT&T Wireless Products Data Book*, AT&T Microelectronics September 1995, pages 11-1 through 11-60.

(3) *Motorola Communications Device Data*, DL136/D REV 4 Q1/96, pages 2-1067 through 2-1088.

(4) *Texas Instruments Data Acquisition Circuits Data Book*, 1995, pages 7-3 through 7-57.

(5) "*IMBE™ and AMBE® Speech Compression*," Digital Voice Systems, Incorporated.

2. Hardware / Pin Information

Table 2-1 shows the pin descriptions broken down into functional groups where possible.

Pin Number	Pin Symbol	Pin Type	Description
98, 99, 2	CH_SEL[2-0]	I	Channel Interface Selection bits
3, 4, 5, 6	BPS_SEL[3-0]	I	Default Bit Rate select bits
90. 89, 88	C_SEL[2-0]	I	A/D-D/A select bits
91	VAD_EN	I	Voice Activation and Detection Enable
92	ECHOCAN_EN	I	Echo Canceller Enable
93	SLEEP _EN	I	Standard Sleep Enable
95	SLIP_EN	I	Slip Enable
37	CLK_I	I	Input Clock
38	CLK_I2	I	Input Clock
40	CLK_O	O	Processor clock output
39	RESETN	I	Reset
43	INT_0	I	Vectored Interrupt 0
46	EPR	O	Encoder Packet Ready
47	DPE	O	Decoder Packet Empty
52, 53, 54, 55, 57, 58	N/C CHP_D[7-2]	 I/O	Channel serial interface - N/C or Channel parallel interface bits 7 through 2
59	CHS_DI CHP_D1	I	Channel serial interface Data input or Channel parallel interface bit 1
60	CHS_I_CLK CHP_D0	I	Channel serial interface input clock or Channel parallel interface bit 0
61	CHS_OBE CHP_OBE	O	Channel serial interface output buffer empty or Channel parallel interface output buffer empty
63	CHS_IBF CHP_IBF	O	Channel serial interface input buffer full or Channel parallel interface input buffer full
64	CHS_O_STRB CHP_RDN	I I/O	Channel serial interface output data strobe or Channel parallel interface output data strobe
65	CHS_I_STRB CHP_WRN	I I/O	Channel serial interface input data strobe or Channel parallel interface input data strobe
67	CHS_SYNC	O	Channel Serial interface sync bit or

Pin Number	Pin Symbol	Pin Type	Description
67 (cont'd)	N/C		Channel parallel interface - no connect
68	CHS_DO CHP_SEL1	O I	Channel serial interface data output or Channel parallel interface select 1
69	CHS_O_CLK CHP_SEL2	I/O I	Channel serial interface output clock or Channel parallel interface select 2
74	CD_SADD	O	Serial Address (used for certain A/D-D/As)
76	H_STOPN	I	Hardware Stop
78	TX_DO	O	Data Output - (to A/D-D/A)
79	TX_STRB	I	Data Output Strobe
80	TX_O_CLK	I/O	Data Output Clock
81	RX_I_CLK	I	Data Input Clock
82	RX_STRB	I	Data Input Strobe
84	RX_DI	I	Data Input (from A/D-D/A)
86	RX_IBF	O	Data Input buffer full
87	TX_OBE	O	Data output buffer empty
45	RESERVED - N/C		
96	RESERVED - N/C		
97	RESERVED - N/C		
8 , 9, 10, 11, 12, 14, 16, 17, 18, 20, 21, 22, 23, 24, 27, 28, 29, 30, 31, 33, 34, 35, 36, 42, 48, 49, 70, 71, 72, 77	N/C		No Connect
7, 19, 26, 50, 56, 66, 85, 100	VDD		Power
1, 13, 15, 25, 32, 41, 44, 51, 62, 73, 75, 83, 94	GND		Ground

Table 2-1 Pin Information

2.1 Definitions

The following section defines several terms that will be used throughout the document.

2.1.1 Passive / Active Modes

The AMBE-1000™ can run in either passive or active modes. In passive mode, data strobes are provided by an external source, while in active mode, data strobes are provided by the vocoder. Both the parallel and serial interfaces can be run in passive and active modes. On the parallel interface, only CHP_RDN and CHP_WRN can be selected as passive or active. On the serial interface, CHS_O_CLK can be selected passive or active.

2.1.2 Advanced Multi-Band Excitation (AMBE®)

The Advanced Multi-Band Excitation (AMBE®) technology is based on the Multi-Band Excitation (MBE) speech model. This speech model provides a unique speech coding framework which results in a number of advantages over linear prediction based speech coders such as CELP, RELP, VSELP, MELP, ECELP, MP-MLQ, and LPC-10, etc. .[(1)]

The AMBE® speech coder (vocoder) was first developed in the mid 1990's by Digital Voice Systems, Incorporated. This vocoder maintains speech intelligibility and naturalness at rates as low as 2.4 kbits/sec. The AMBE® system is less complex than either CELP or VSELP, and therefore, it has been integrated into a low-cost, low-power integrated circuit, the AMBE-1000™. Finally, the AMBE® speech coder can be easily scaled to virtually any data rate above 2.4 kbits/sec.

See reference (5) for further details.

2.2 Channel Interface: Serial / Parallel Select

Three I/O pins determine whether the channel interface will operate in parallel or serial mode. These bits are CH_SEL0, CH_SEL1, and CH_SEL2 (TQFP pins 2,98 and 99). Table 2.2 -1 shows the configuration of the different interfaces.

CH_SEL2	CH_SEL1	CH_SEL0	Interface type	Passive / Active
0	0	0	Parallel	CHP_RDN and CHP_WRN *Passive*
0	0	1	↓	CHP_RDN and CHP_WRN *Active*
0	1	0	serial	Packetized Serial CHS_I_CLK *Passive* / CHS_O_CLK *Active*
0	1	1		Packetized Serial CHS_I_CLK and CHS_O_CLK *Passive*
1	0	0		Unformatted Serial (self Sync on) 1 bit per baud CHS_I_CLK and CHS_O_CLK *Passive*
1	0	1		Unformatted Serial (self Sync on) 2 bits per baud CHS_I_CLK and CHS_O_CLK *Passive*
1	1	0		Unformatted Serial (self Sync on) 3 bits per baud CHS_I_CLK and CHS_O_CLK *Passive*
1	1	1	↓	Unformatted Serial (self Sync on) 4 bits per baud CHS_I_CLK and CHS_O_CLK *Passive*

Note: CHP_RDN: Parallel Output Data Strobe
CHP_WRN: Parallel Input Data Strobe
CHS_I_CLK: Input Clock
CHS_O_CLK: Output Clock

Table 2.2-1 Channel interface pin settings

When the parallel channel interface is selected, channel data is sent and received via the 8-bit CHP_D I/O bus (CHP_D7 through CHP_D0, collectively), pins 52-55 and 57-60. When the serial channel interface is selected, channel data is received on pin 59 CHS_DI and sent out on pin 68 CHS_DO.

Section 3.2.2, Unformatted serial, will explain “bits per baud.”

2.3 A/D-D/A I/O and Companding Configuration

The AMBE-1000™ can be configured to interface with most linear, A-law, and μ-law A/D-D/A (codec) chips. The following A/D-D/A’s are supported and shown in Table 2.3-1. The A/D-D/A type can be modified using command interface packets (see section 3.1.1.4).

For the A/D-D/A’s shown in the table, no additional control download is required to the A/D-D/A chip via the AMBE-1000™.

A/D-D/A	C_SEL2	C_SEL1	C_SEL0	Type
Generic μ-Law	0	0	0	μ-Law
Generic A-Law	1	0	0	A-Law
AT&T CSP1027 (Mic In)	0	0	1	Linear
AT&T CSP1027 (Aux In)	1	0	1	Linear
TI TLC32046 A/D-D/A	0	1	0	Linear
Generic 16 bit Linear	1	1	1	Linear

Note: Contact DVSI if there is a question about a particular manufacturer's A/D-D/A.

Table 2.3-1 A/D-D/A pin configuration

The AMBE-1000™ is compatible with many Texas Instruments A/D-D/A. If you are using a TI linear A/D-D/A with an equivalent interface to the TLC32046, you should be able to use the C_SEL pins with the TI setting. Please look at Appendix section 1.5.3, for the particular device that you have selected, you will probably have to change some control register settings. Contact DVSI if you have questions about the TI A/D-D/A chip that you are using. We will advise you on the proper interface to the AMBE-1000™.

After configuring the C_SEL bits to the appropriate setting, configuration data may be sent to the A/D-D/A by sending a special packet to the AMBE-1000™. The description of the special packet and the interface circuit are shown in the appendix.

The A/D-D/A chip that is selected will determine the AMBE-1000™'s A/D-D/A interface. Table 2.3-2 shows the **required** pins needed for the A/D-D/A interface. TX_O_CLK can be either an input or an output depending on the configuration.

Pin Symbol	Pin Type	Pin number	Description
TX_DO	O	78	Data Output - (to A/D-D/A)
TX_STRB	I	79	Data Output Strobe
TX_O_CLK	I/O	80	Data Output Clock
RX_I_CLK	I	81	Data Input Clock
RX_STRB	I	82	Data Input Strobe
RX_DI	I	84	Data Input (from A/D-D/A)

Table 2.3-2 AMBE-1000™ A/D-D/A pins

2.4 Bit Rate

The AMBE-1000™ can support bit rates between 2400 and 9600 bps. The Total Rate is the combination of the Speech rate and the Forward Error Correction (FEC) rate. The AMBE-1000™ has the flexibility to change the speech and FEC rates in 50 bps increments. High FEC rates enable

the vocoder to maintain good quality speech even at BER rates as high as 5%. This is a feature that is ideal for many mobile communication applications that experience degraded channel conditions.

Forward error correction is used when the user anticipates a degraded channel with significant bit errors. The default bit rate (the bit rate after reset) is selected based on the settings of pins BPS_SEL3 - BPS_SEL0. Table 2.4-1 shows the most common speech and FEC rates and the AMBE-1000™ can be set to these **default configurations**. If an application requires a different speech rate and FEC rate from the ones that are listed, please contact DVSI to determine the appropriate configuration of the vocoder.

The AMBE-1000™'s FEC rate and speech rate can change from the default setting by sending the appropriate Command packets after reset. This is explained in detail in section 3.1.1.4.

BPS_ SEL3	BPS_ SEL2	BPS_ SEL1	BPS_ SEL0	Speech Rate	FEC Rate	Total Rate
0	0	0	0	2400 bps	0	2400 bps
0	0	0	1	3600 bps	0	3600 bps
0	0	1	0	3600 bps	1200 bps	4800 bps
0	0	1	1	4800 bps	0	4800 bps
0	1	0	0	9600 bps	0	9600 bps
0	1	0	1	2350 bps	50 bps	2400 bps
0	1	1	0	4850 bps	4750 bps	9600 bps
0	1	1	1	4550 bps	250 bps	4800 bps
1	0	0	0	3100 bps	1700 bps	4800 bps
1	0	0	1	4400 bps	2800 bps	7200 bps
1	0	1	0	4150 bps	2250 bps	6400 bps
1	0	1	1	3350 bps	250 bps	3600 bps
1	1	0	0	7750 bps	250 bps	8000 bps
1	1	0	1	4650 bps	3350 bps	8000 bps
1	1	1	0	3750 bps	250 bps	4000 bps

Table 2.4-1 Pin configuration for bit rate

3. Channel Interface

The AMBE-1000™ operates with a 20 millisecond frame size. This requires channel data to be sent to the decoder and received from the encoder every 20 milliseconds.

As stated in the previous section the channel interface can be configured as a parallel interface or a serial interface based on the pin configuration. The parallel and serial interface can operate in a

packetized format and a description of this is in the following sections. Only the serial channel interface can operate in an unformatted mode.

3.1 Parallel

In this mode an 8-bit bi-directional parallel interface is used to communicate with the AMBE-1000™. Table 3.1-1 shows the **required** pins needed for the Parallel Channel interface.

Pin Symbol	Pin Type	Pin Number	Description
EPR	O	46	Encoder Packet Ready
DPE	O	47	Decoder Packet Empty
CHP_D[7-0]	I/O	52, 53, 54, 55, 57, 58, 59, 60	Channel parallel interface bits 7 through 0
CHP_OBE	O	61	Channel parallel interface output buffer empty
CHP_IBF	O	63	Channel parallel interface input buffer full
CHP_RDN	I/O	64	Channel parallel interface output data strobe
CHP_WRN	I/O	65	Channel parallel interface input data strobe
CHP_SEL1	I	68	Channel parallel interface select 1
CHP_SEL2	I	69	Channel parallel interface select 2

Table 3-1 Parallel Channel Interface Pin Information

CHP_SEL1 and **CHP_SEL2** (pins 68 and 69), should be tied to ***ground*** if running in passive parallel mode. If running in active parallel mode, these pins should be ***no connects.***

3.1.1 Packetized Parallel

Packets are sent to or received from the AMBE-1000™ 8 bits at a time over the parallel interface. The AMBE-1000™ expects to receive the packet data **high byte first**. Figure 3.1.1-1a shows the basic frame format which allows a total of 34 bytes of information which contain control and voice data to be sent every frame. This structure allows certain control information to be changed while voice data continues to be processed. The AMBE-1000™ allows data rates to change and features to be enabled, that were not originally set from the default pin configuration. The control information that will be allowed to change in this manner is discussed in sections 3.1.1.2 and 3.1.1.4.

Figure 3.1.1-1b shows a control frame structure that can be sent to the vocoder. The 48 bit control area is the same as that shown in figure 3.1.1-1a, the control data area is explained in a later section.

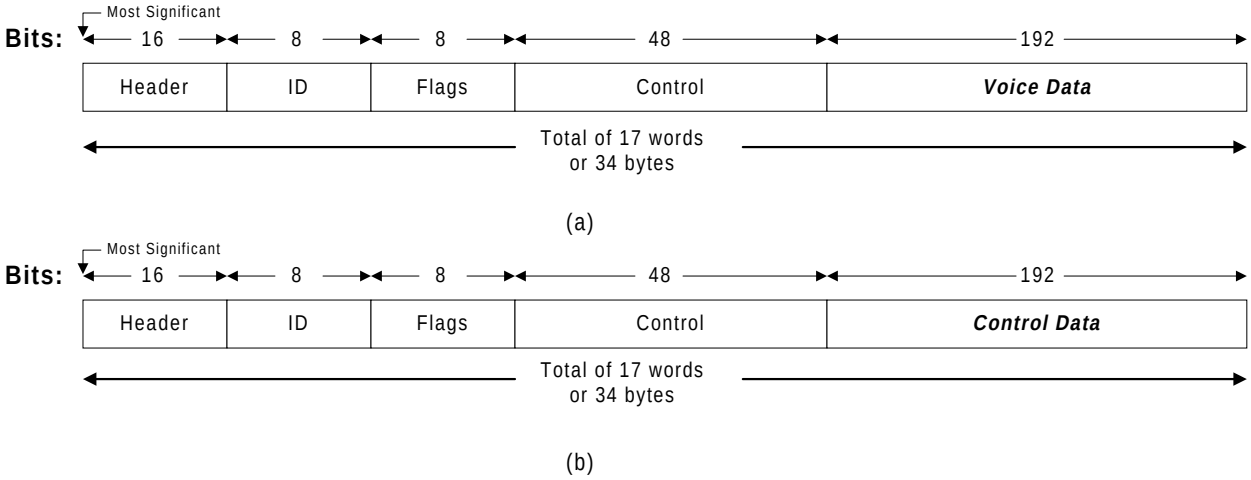
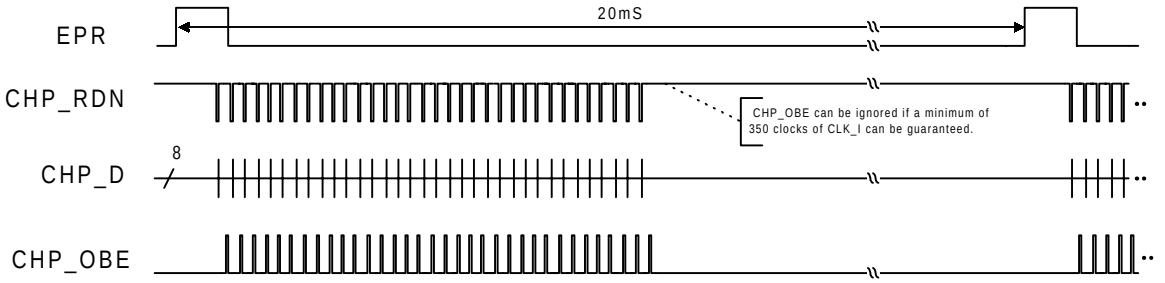


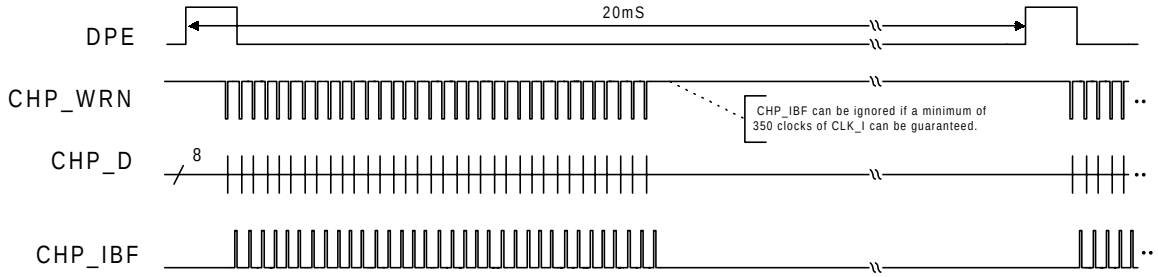
Figure 3.1.1-1 Basic Frame format

In packetized mode the frame packet is 17 words (34 bytes) in length, when the voice data (or control data) is less than 192 bits (12 words = 9600 bps), the user **must pad** the packets so that the number of words sent to the AMBE-1000™ is 17.

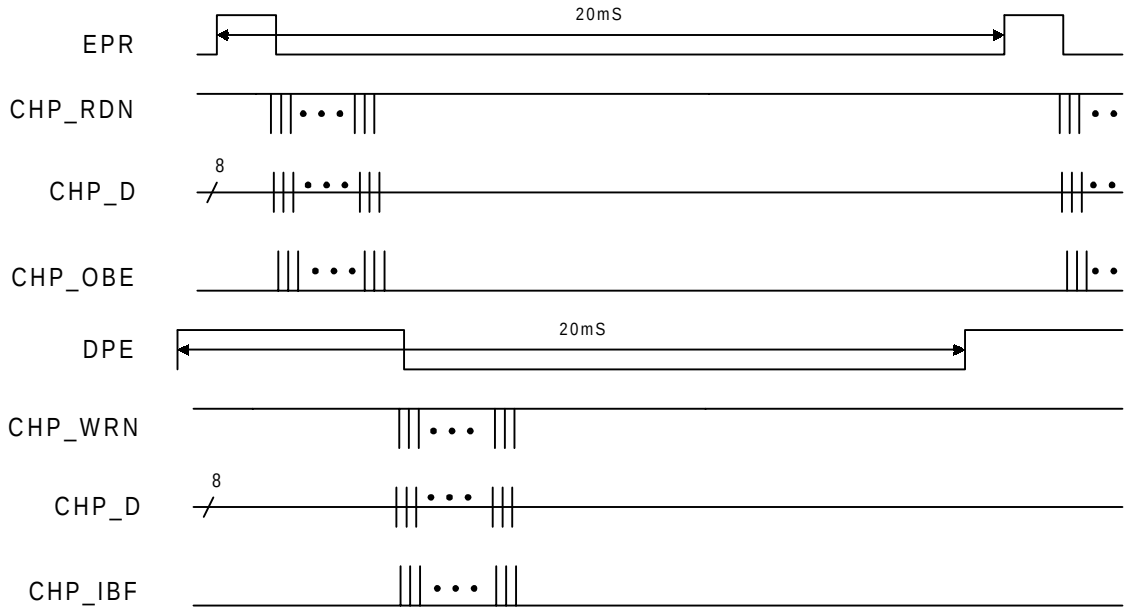
Figure 3.1.1-2 shows the high level timing diagram for the Passive Parallel mode. Figure 3.1.1-2 a and b shows the encoder and decoder signals separate for clarity. Figure 3.1.1-2 c shows the encoder and decoder signals together, the way they might appear on a logic analyzer (***NOTE***: **CHP_D** is shown twice in (c)) Figure 3.1.1-2 (c) may look different if your software allows the decoder to send information to the AMBE-1000™ first and read encoded information second. This could be the case since the AMBE-1000™ upon power-up has the **DPE** signal high and the **EPR** signal low. This will depend on how the AMBE-1000™ is connected to the controller.



(a) Encoder



(b) Decoder



(c) Encoder and Decoder together.

Figure 3.1.1 -2 High level timing diagrams for ***Passive*** Parallel Packetized Mode

Figure 3.1.1-3 shows the basic input and output timing for passive packetized parallel mode. It should be noted that the passive channel parallel port is asynchronous. Figure 3.1.1.-3 (a) is a timing relationship diagram of the passive parallel channel input. When the decoder packet empty (DPE) goes high, this signals that this interface is ready to receive the next frame (34 bytes) of decoder

channel data. This data will be sent in bytes in the format shown in figure 3.1.1.-1. After each byte is sent, the host must wait for the channel parallel input buffer full (CHP_IBF) to transition low before the next byte is sent. This process continues until all 34 bytes are sent to the AMBE-1000™.
CHP_IBF can be ignored if the time between CHP_WRN pulses is at least 350 cycles of CLK_I.

Figure 3.1.1.-3 (b) shows the timing relationship of the passive parallel channel output. When the encoder packet ready (EPR) goes high, this indicates that an encoder packet is ready to be transmitted over the parallel channel interface. As stated in the previous paragraph, the data will be sent from the AMBE-1000™ in the format shown in figure 3.1.1-1. After each byte is sent, the host must wait until the channel parallel output buffer empty (CHP_OBE) to transition low before the next byte can be read. Again, this process will continue until all 34 bytes are read from the AMBE-1000™.
CHP_OBE can be ignored if the time between CHP_RDN pulses is at least 350 cycles of CLK_I.

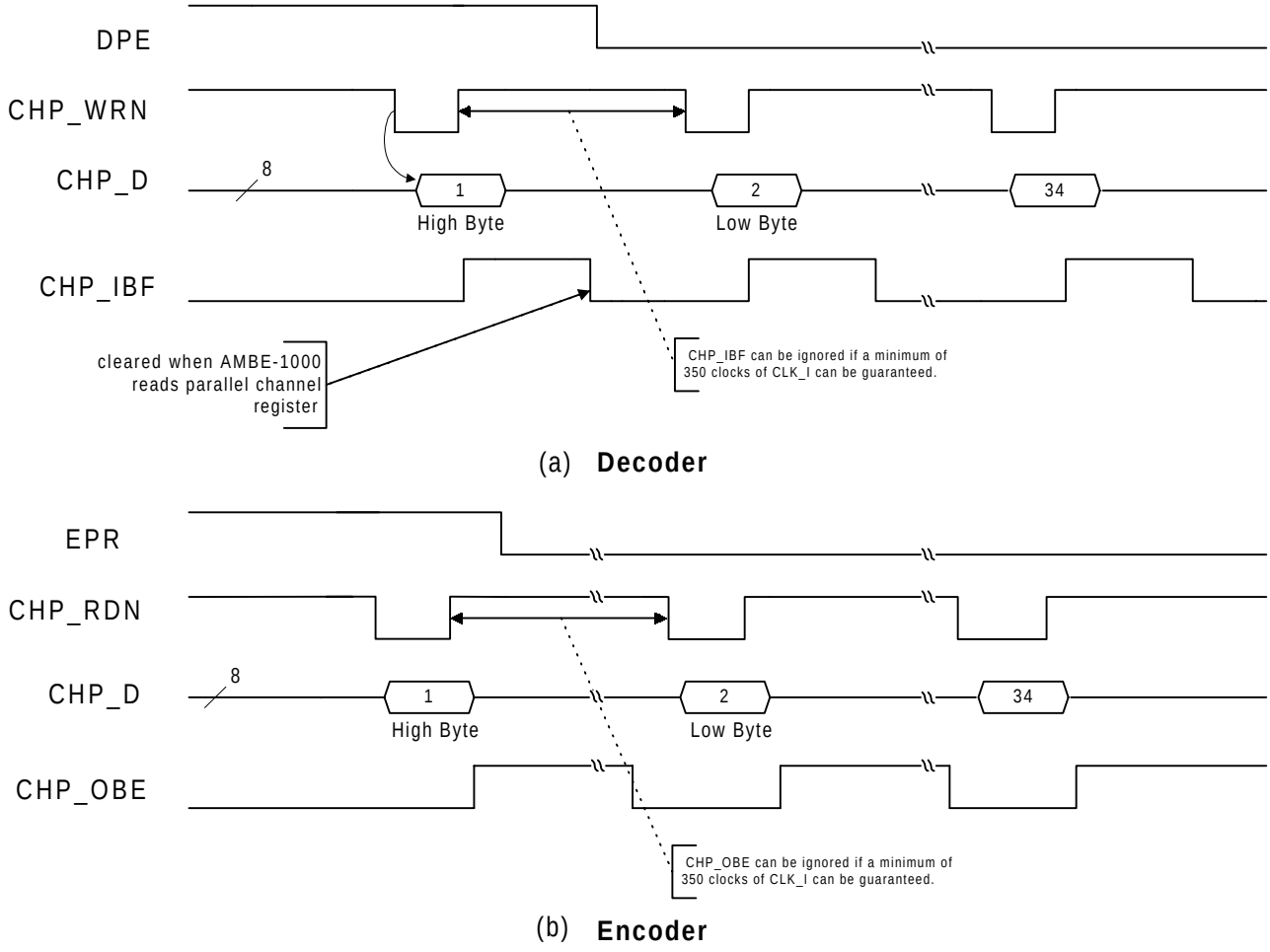
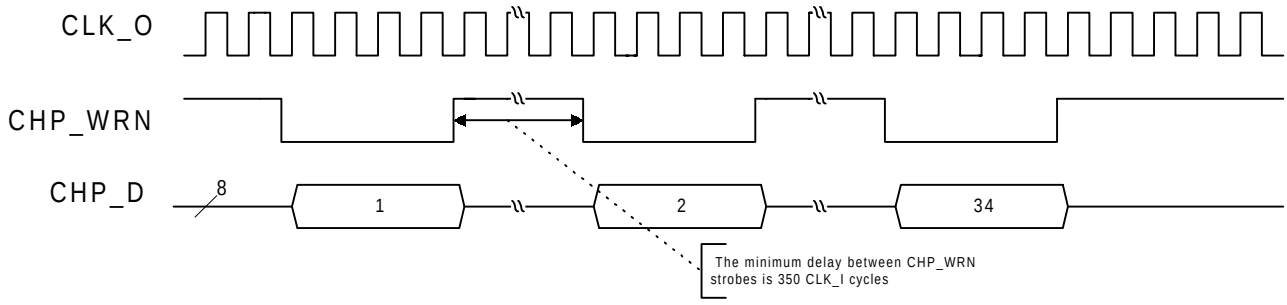


Figure 3.1.1 -3 ***Passive*** Parallel Packetized Mode timing diagram

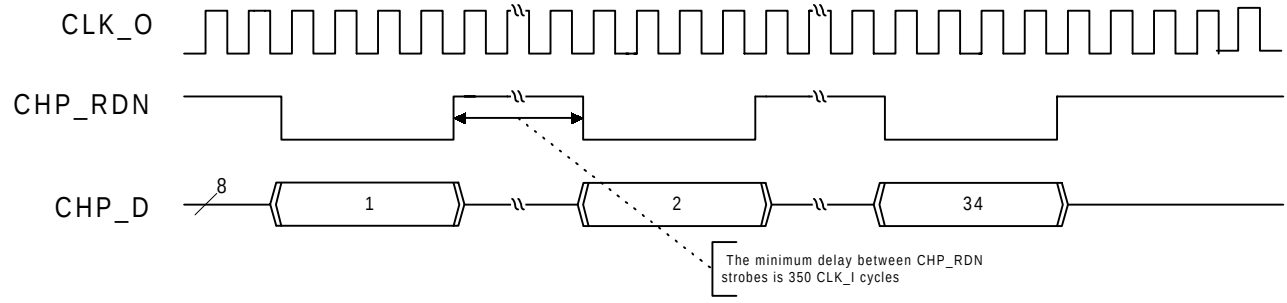
Figure 3.1.1-4 shows the basic input and output timing for the active packetized parallel mode. In this configuration the AMBE-1000™ is in control of the interface. Every 20 milliseconds a series of CHP_WRN and CHP_RDN strobes will begin. There will be 34 CHP_WRN strobes to receive decoder channel data. The same will apply for encoder data that is sent to the channel.

Figures 3.1.1-4 (a) shows the timing relationship of the active parallel channel output port (from the encoder). It should be noted that the CHP_WRN pulse width is 4 CLK_O cycles in length and there will be a minimum delay of 350 CLK_I cycles before the next data word is placed on the channel. CLK_O is the buffered clock of CLK_I. Therefore, CLK_O minus some delay is equal to CLK_I.

Figure 3.1.1-4 (b) is the timing relationship of the active parallel channel input port (to the decoder). Like CHP_WRN, CHP_RDN's pulse width is 4 CLK_O cycles in length and there will be a minimum delay 350 CLK_I cycles before the next byte of data is read from the channel.



(a) Decoder



(b) Encoder

Figure 3.1.1-4 ***Active*** Packetized Parallel Mode timing diagram

3.1.1.1 Header

The header is a unique 16 bit word that precedes the packetized frame data. The header word **MUST** be **0x13EC**. A correct header indicates that the current frame is valid. In packetized operation, the header word is used for synchronization of the frame.

Header = 0x13EC

3.1.1.2 Flags

The flag bits are the lower 8 bits of the second word in the packet, shown in figure 3.1.1.2-1, and have the following two purposes:

1.) To report status of certain functions from the AMBE-1000™.
2.) To inform the AMBE-1000™ about the data it is receiving.

The *Lost flag* (shown in figure 3.1.1.2-1) is an example of the second case. When the host processor or controller sets this flag, it is informing the AMBE-1000™ that the data field it is currently receiving is not valid and must be ignored.

The other five flags are from the AMBE-1000™, these flags indicate whether those functions are active in the current frame.

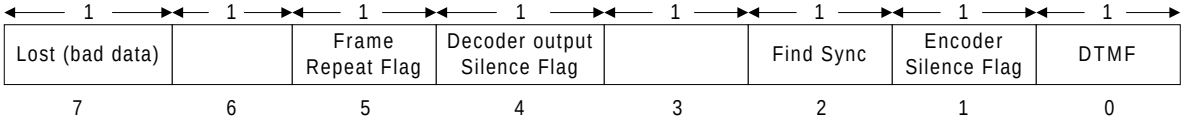


Figure 3.1.1.2-1 Status Flags

The *DTMF flag* will be set when the encoder detects a DTMF tone. When this happens the second control word will contain the DTMF code and amplitude(figure 3.1.1.2-2). Table 3.1.1.2-1 shows the DTMF codes.

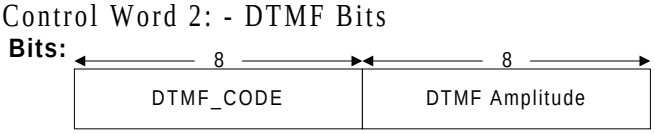


Figure 3.1.1.2-2 DTMF bits

DTMF Digit	DTMF CODE
1	0x00
2	0x04
3	0x08
4	0x01
5	0x05
6	0x09
7	0x02
8	0x06
9	0x0a
0	0x07
*	0x03
#	0x0b
A	0x0c
B	0x0d
C	0x0e
D	0x0f

Table 3.1.1.2-1 DTMF Codes

The *encoder silence flag* is set when the encoder detects a silence frame and Voice Activation and Detection (VAD) is enabled. When this occurs the voice data part of the packet will contain a silence frame with comfort noise insertion (CNI).

The *find sync flag* is enabled when the AMBE-1000™ is in unformatted mode and is looking for the synchronization bit which indicates the beginning of a frame.

The *decoder output silence flag* is set after the AMBE-1000™ is told that the previous incoming decoder packet contained a silence frame. As stated previously, a decoder packet with an ID = 0x03 can enable certain features of the AMBE-1000™. When *decoder input silence flag* is set in AMBE-1000™ word 1 in the speech configuration with A/D-D/A control packet, the *decoder output silence flag* will be set during the next encoder output frame. The *decoder output silence flag* is used to let the host know that the AMBE-1000™ received the decoder silence frame.

If the host processor/controller knows that the data that it is sending is corrupted, the host can set the *lost flag* (lost flag = 1). This will tell the AMBE-1000™ not to process the voice data. Also in the next encoded packet received from the AMBE-1000™, the *frame repeat flag* will be set. *The lost flag should be set when changing the number of total bits per frame using the speech configuration with voice data packet.*

The *frame repeat flag* will also be set if the decoder detects too many errors in the voice data area.

3.1.1.3 ID and their Packet Descriptions

The AMBE-1000™ will perform various functions based on the value of the ID field. As shown in figure 3.1.1 the ID field is the upper 8 bits of the second word of the packet. Table 3.1.1.3-1 shows the various ID's that are allowed and a brief description of each.

ID	Type	Description
0x00	Data Only	In this mode flags will be sent and received by the AMBE-1000™, but no control information will be read from the frame data. Control information and flags are discussed in the following sections.
0x01	Speech Configuration with Voice data	Voice data and control information will be sent to the vocoder.
0x02	Additional Speech Configuration with Voice data	Voice data with additional control information will be sent to the vocoder.
0x03	Speech Configuration with A/D-D/A Control data	A/D-D/A control information will be in the voice data area.
0x04	Low Power Mode	When this mode is activated the AMBE-1000™ will go into a mode where no voice packets are being processed.
0x06	Dual Tone generation	Special mode, will tell the decoder to generate the following Dual Tone. (see section 6 for more details)
0xFE	Wake up Packet	Used to wake up the AMBE-1000™ from Standard Sleep Mode (see Section 7 for a description of Standard Sleep Mode

Table 3.1.1.3-1 ID field descriptions

Tables 3.1.1.3-3 and 3.1.1.3-4 shows example frame packets of each of the above ID types. The next few paragraphs will explain each of the ID types in more detail.

The ***data only*** ID (**0x00**) will be the usual ID when data is sent from/to the AMBE-1000™. The first column of Table 3.1.1.3-3 shows an example of a data only frame packet. The "don't cares" after the control words are the compressed voice data bits.

The ***Speech configuration with voice data*** (**0x01**) is typically sent to the AMBE-1000™ when changes to the bit rate and/or the FEC rate are required. These changes can be made to the AMBE-1000™ at the same time that it is required to process voice data, the data will be processed with changes the user has specified. See section 3.1.1.4 for more information about the control words.

Additional speech configuration with voice data (**0x02**) is used to send AMBE-1000™ input/output volume information and the silence threshold value used by the voice activation and detection (VAD) algorithm. Table 3.1.1.3-2 shows the input/output volume relationships. The input volume bits are the upper 8 MSB's of control word 1. There is a log relationship between the input volume bits and the input volume. The input volume bits can range from -128 (lowest) to +127 (highest) and each bit

is worth .75 dB. The input volume normal setting is 0. There is a linear relationship between the output volume bits and the output volume. The output volume is the lower 8 bits of control word 1 and can range from 0 (lowest) to 256 (highest). The output volume normal setting is 128. The silence threshold value as the name implies, is the threshold point that the voiced energy has to be above to be a non-silence frame. DVSI recommends that the silence threshold value be 500 (0x1F4).

Input		Output	
127	**95.25 dB**	255	**Max. Output**
10	**7.5 dB**		
0	**0 dB**	128	**Typical**
10	**-7.5 dB**		
-127	**-96 dB**	0	**No volume**

Table 3.1.1.3-2 Input/ Output Volume relationships

	Data Only	Speech Configuration with Voice Data	Additional Speech Configuration with Voice data
Header	0x13ec	0x13ec	0x13ec
ID/Flags	0x0000	0x0100	0x0200
Control 1	0x0000	Control word 1	Input Vol. / Out Vol.
Control 2	0x0000	Control word 2	Silence Threshold
Control 3	0x0000	0x0000	0x0000
↑	0xXXXX	0xXXXX	0xXXXX
|	0xXXXX	0xXXXX	0xXXXX
Voice data	0xXXXX	0xXXXX	0xXXXX
if required	0xXXXX	0xXXXX	0xXXXX
|	0xXXXX	0xXXXX	0xXXXX
|	0xXXXX	0xXXXX	0xXXXX
|	0xXXXX	0xXXXX	0xXXXX
|	0xXXXX	0xXXXX	0xXXXX
|	0xXXXX	0xXXXX	0xXXXX
|	0xXXXX	0xXXXX	0xXXXX
|	0xXXXX	0xXXXX	0xXXXX
↓	0xXXXX	0xXXXX	0xXXXX

Table 3.1.1.3-3 Example packets with different ID fields

	Speech Configuration with A/D-D/A Control	Low Power Mode	DTMF	Wake-up
Header	0x13ec	0x13ec	0x13ec	0x13ec
ID/Flags	0x0300	0x0400	0x0600	0xfe80
Control 1	0x03c8	0x0001	0x55c0	0x0000
Control 2	0x0000	0x000c	0x55c0	0x0000
Control 3	0xfffd	0x0000	0x26d0	0x0000
Control 4	0x1ec0	0x40d0	0x1b43	0x0000
Control 5	0x4020	0xc0d0	0x0000	0x0000
Control 6	0x800f	0x8000	0x0000	0x0000
Control 7	0xd000	0x40c0	0x0000	0x0000
Control 8	0x0000	0x2710	0x0000	0x0000
Control 9	0x0000	0x00d0	0x0000	0x0000
Control 10	0x0000	0x0000	0x0000	0x0000
Control 11	0x0000	0x0000	0x0000	0x0000
Control 12	0x0000	0x0000	0x0000	0x0000
Control 13	0x0000	0x0000	0x0000	0x0000
Control 14	0x0000	0x0000	0x0000	0x0000
Control 15	0x0000	0x0000	0x0000	0x0000

Table 3.1.1.3-4 More Packet examples with different ID's

Speech configuration with A/D-D/A control information (**0x03**), shown in Table 3.1.1.3-3, is typically used at power-up or reset when certain programmable features of the A/D-D/A chip are to be programmed **OR** when AMBE-1000™ features are to be enabled. Currently, the AMBE-1000™ supports a variety of A/D-D/A's from manufacturers like Motorola, Texas Instruments, and AT&T. If AT&T's CSP1027 is chosen, the pin configuration shown in Table 2.3-1 will program the A/D-D/A to the required state. The 0x03 ID type will allow you to update/change the programmable features of the CSP1027. Table 3.1.1.3-5 illustrates the details of 0x03 ID packet and the two input modes of the CSP1027. Note that Control words 1 through 3 are in the control field and Control words 4 through 15 are in the control data field.

IMPORTANT NOTE: In order to program any of the programmable features of any A/D-D/A chip, the AMBE-1000™ must be placed into **Standard Sleep Mode first**. The AMBE-1000™ can be placed into Standard Sleep Mode upon power up or reset by enabling (=1) the **SLEEP_EN pin (pin 93)** or by sending the **Standard Sleep Mode command packet** (see section 7). Once the vocoder is in Standard Sleep mode, the speech configuration with A/D-D/A control can be sent. The **wake-up packet (ID = 0xFE) must be sent** in order to place the AMBE-1000™ back into normal operating mode.

Figure 3.1.1.3-5 shows the bit information for the Control 2 (AMBE-1000™ word 1). This word can enable and disable specific features of the AMBE-1000™.

The ***compand flag*** (bit 9 = "1") together with the ***A-law flag*** (bit 8 = "1") will enable A-law companding on the A/D-D/A serial interface. If the ***A-law flag*** is a "0", μ-law companding will be sent on the A/D-D/A serial interface. To enable the Texas Instruments (TI) A/D-D/A interface bit 9 must be a "0" and bit 8 must be a "1". If you are using a TI programmable A/D-D/A (meaning certain control registers must be set), the remainder of this packet must contain TI register information and the AMBE-1000™ word 1 must also be enabled for TI, see Appendix 1.5.3 for an example packet. This type of packet information must be sent to the AMBE-1000™ while the vocoder is in standard sleep mode. Also, if the A/D-D/A is programmable and a register change is required, the AMBE-1000™ must be in standard sleep mode and a ID = 0x03 must be sent the AMBE-1000™ to change the A/D-D/A information.

Bit 1, the ***decoder input silence flag***, will tell the AMBE-1000™ to send out a silence frame to the A/D-D/A chip.

Bits 11 and 12 can selectively enable (1) or disable (0) the echo canceller and the voice activation and detection, respectively. Also if the decoder silence flag is enabled, the decoder will also disregard the voice data for this frame and output silence with background comfort noise. The bit types mentioned in this paragraph can be enabled or disabled at any time.

Self Sync flag (bit 15) is only used in unformatted data mode. This enables the AMBE-1000™ to begin the self synchronization process with the channel interface.

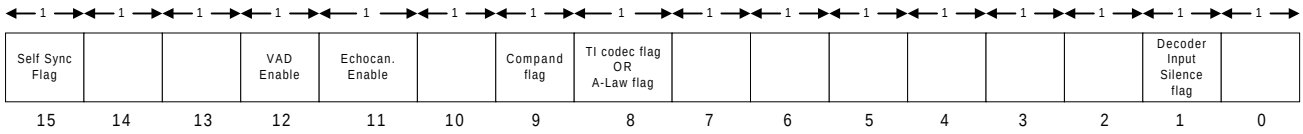


Figure 3.1.1.3-5 Control 2 (AMBE-1000™ Word 1)

The wake-up packet (ID=0xFE) only has to be sent to the AMBE-1000™ if the vocoder is in standard sleep mode. If the vocoder is in any other low power mode, either a channel interrupt or a reset will wake-up the vocoder. The type of interrupt used will depend on which low power mode you are using. Low power modes are discussed in further detail in Section 7.

Parameter	Microphone input	Auxiliary input	
Header	0x13ec	0x13ec	
ID / Flags	0x0300	0x0300	
Control 1 (AMBE-1000™ word 0)	0x03c8	0x03c8	Control Data
Control 2 (AMBE-1000™ word 1) [Enable AMBE-1000™ features]	0x0000	0x0000	Flags
Control 3 (AMBE-1000™ word 2) [One minus the number of words sent to the A/D-D/A After this point]	0xfffd	0xfffd	Control Data 1 - 4 = -3
Control 4 (CIOC0)	0x1ec0	0x1ea0	A/D-D/A Reg.
Control 5 (CIOC1)	0x4020	0x4020	A/D-D/A Reg.
Control 6 (CIOC2)	0x800f	0x800f	A/D-D/A Reg.
Control 7 (CIOC3)	0xd000	0xd000	A/D-D/A Reg.
Control 8	0x0000	0x0000	|
Control 9	0x0000	0x0000	|
Control 10	0x0000	0x0000	|
Control 11	0x0000	0x0000	|
Control 12	0x0000	0x0000	|
Control 13	0x0000	0x0000	|
Control 14	0x0000	0x0000	|
Control 15	0x0000	0x0000	↓

Values for CIOC registers can be different.

These values are sent when the appropriate codec configuration is selected

Table 3.1.1.3-5 Detailed example of a speech Configuration with A/D-D/A control packet for AT&T's CSP1027

3.1.1.4 Control

The Control part of the frame packet shown in figure 3.1.1-1, shows that 48 bits or 3 words have been assigned for passing information to and from the vocoder. Table 3.1.1.4-1 show the possible data control configurations of the AMBE-1000™.

The different configurations of the Speech and FEC rates are shown in Table 3.1.1.4.-1. The rates shown in the table can be programmed by setting the proper BPS_SEL pins or a sending software configuration packet. If higher FEC rates are required for your system contact DVSI to determine the best configuration of the vocoder.

Control Word1	Control Word2	Speech Rate	FEC Rate	Total Rate
0x4130	0x0000	2400 bps	0	2400 bps
0x6148	0x0000	3600 bps	0	3600 bps
0x6160	0x9006	3600 bps	1200 bps	4800 bps
0xa360	0x0000	4800 bps	0	4800 bps
0xe4c0	0x0000	9600 bps	0	9600 bps
0x4130	0x0001	2350 bps	50 bps	2400 bps
0xa3c0	0xf200	4850 bps	4750 bps	9600 bps
0xa360	0x0020	4550 bps	250 bps	4800 bps
0x5160	0x9400	3100 bps	1700 bps	4800 bps
0xa390	0x9800	4400 bps	2800 bps	7200 bps
0xa380	0x9600	4150 bps	2250 bps	6400 bps
0x5148	0x0020	3350 bps	250 bps	3600 bps
0xe4a0	0x0020	7750 bps	250 bps	8000 bps
0xa3a0	0x9a00	4650 bps	3350 bps	8000 bps
0x6150	0x0020	3750 bps	250 bps	4000 bps

Table 3.1.1.4-1 Speech and FEC rates

Control word 3 will display the error rate of the decoder. This error rate is the average of the total number of bit errors detected over approximately the last 100 frames. The decoder will only display this information when FEC is enabled and it will be displayed ever frame.

The following equation shows how to calculate the Bit Error Rate (BER).

$$\sim \text{BER} = \frac{\text{The total number of errors reported}}{\text{The total bps rate} * 0.02}$$

This will give you the total number of bits per frame.

3.1.1.5 Data

3.1.1.5.1 Voice

Figure 3.1.1.5.1-1 shows the voice data portion of the packet. For a total data rate of 9600 bps all 192 voice data bits are utilized. For rates less than 9600 bps, only the most significant N bits are utilized where N is the number of bits per frame. **PLEASE NOTE, in packetized mode** when using frames with less than 192 bits of voice data, the user **MUST** "pad" the packet such that the number of voice data bits is 192 (12 words). The used bits should be filled with 0's. The MSB's contain the valid bits. In packetized mode the AMBE-1000™'s packet frame size is 17 words (34 bytes).

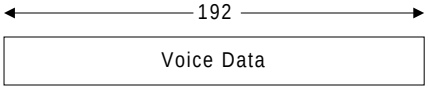


Figure 3.1.1.5.1-1 Part of Frame Packet, Voice Data

3.1.1.5.2 A/D-D/A Control Data

Figure 3.1.1.5.2-1 shows the control data portion of the packet. Remember that the control data part of the packet can only be utilized when using packet **ID type 0x03**.

In the Speech Control Configuration with A/D-D/A Control Data, the host processor or controller will be able to send the AMBE-1000™ A/D-D/A control information. **PLEASE NOTE, in packetized mode** when using frames with less than 192 bits of control data (which is the case in the example packet in Table 3.1.1.2-5), the user **MUST** pad the packet such that the number of control data bits is 192 (12 words). In packetized mode the AMBE-1000™ packet frame size is 17 words (34 bytes).

This control data format provides a means of supporting other manufacturer's A/D-D/A chips. Please refer to the appendix to see several example packets.

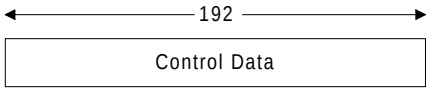


Figure 3.1.1.5.2-1 Part of Frame Packet, Voice Data

3.2 Serial

Processed encoded data is sent to the channel via CHS_DO and encoded data is received from the channel via CHS_DI and processed by the decoder. Table 3.2-1 shows the **required** pins needed for the Serial Channel interface.

Pin Symbol	Pin Type	Pin Number	Description
EPR	O	46	Encoder Packet Ready
DPE	O	47	Decoder Packet Empty
CHS_DI	I	59	Channel serial interface Data input
CHS_I_CLK	I	60	Channel serial interface input clock
CHS_OBE	O	61	Channel serial interface output buffer empty
CHS_IBF	O	63	Channel serial interface input buffer full
CHS_O_STRB	I	64	Channel serial interface output data strobe
CHS_I_STRB	I	65	Channel serial interface input data strobe
CHS_SYNC	O	67	Channel Serial interface sync bit
CHS_DO	O	68	Channel serial interface data output
CHS_O_CLK	I/O	69	Channel serial interface output clock (Output when in Active Mode)

Table 3.2-1 Serial Channel Interface Pin Information

3.2.1 Packetized Serial

3.2.2 Packetized Serial Input

Figure 3.2.2-1 shows the timing for the decoder input when the channel is configured for the passive packetized mode. A low-to-high transition of the decoder packet empty flag (DPE) will signal the AMBE-1000™ is ready to accept a packet from the serial channel interface. In this mode, an externally generated bit clock (CHS_I_CLK) synchronizes all events occurring within the channel. The maximum frequency of CHS_I_CLK is $\frac{1}{2}$ the input frequency of CLK_I. Therefore, if CLK_I is running at 30 MHz, the maximum frequency of CHS_I_CLK is 15 MHz.. A high-to-low transition of the channel input strobe (CHS_I_STRB) followed by the next rising edge of CHS_I_CLK initiates the start of an input transaction. The first serial data is read from CHS_DI on the ***next rising*** edge of CHS_I_CLK. Once the 16 bit data word is read, the channel serial input buffer full flag (CHS_IBF) will transition high indicating to the channel that the last word sent to the AMBE-1000™ has not been read. The AMBE-1000™ cannot accept another word from the channel until the CHS_IBF transitions low. The AMBE-1000™ will service the interrupt within the next 350 cycles of CLK_I. CHS_IBF can be ignored if there are at least 350 cycles of CLK_I between successive CHS_I_STRB's. After the AMBE-1000™ services the interrupt and reads the first word, DPE will transition low. The AMBE-1000™ expects 16 more words from the channel interface to create a 17 word frame packet.

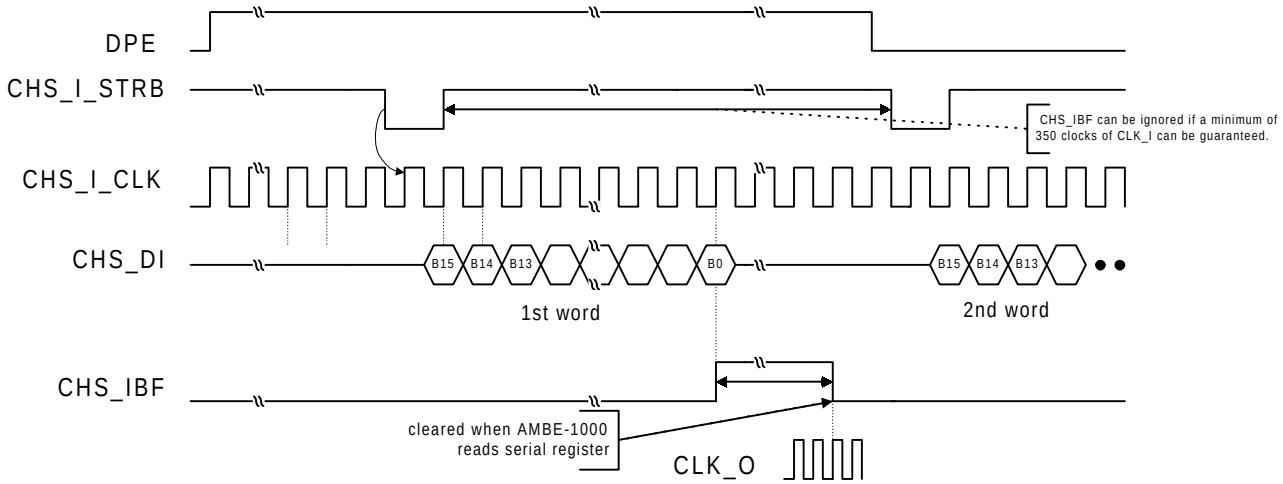


Figure 3.2.2-1 Decoder Passive mode timing

3.2.3 Packetized Serial Output

Figure 3.2.3-1 shows the timing for the encoder output when the channel is configured for passive packetized mode. A low-to-high transition of the encoder packet ready flag (EPR) will signal the AMBE-1000™ is ready to send a packet to the serial channel interface. In this mode, an externally generated bit clock (CHS_O_CLK) synchronizes all events occurring within the channel. The maximum frequency of CHS_O_CLK is $\frac{1}{2}$ the input frequency of CLK_I. Therefore, if CLK_I is running at 30 MHz, the maximum frequency of CHS_O_CLK is 15 MHz. A high-to-low transition of the channel output strobe (CHS_O_STRB) followed by the next rising edge of CHS_O_CLK initiates the start of an output transaction. On this ***first rising edge*** of CHS_O_CLK, the first serial data bit is sent to CHS_DO. CHS_OBE transitions high to indicate that the output buffer is empty. Therefore, the controller should read the CHS_DO data on the ***falling edges*** of CHS_O_CLK. The controller **must** not strobe for another word of data until CHS_OBE transitions low, indicating that there is data in the AMBE-1000™ serial output port. CHS_OBE can be ignored if there are at least 350 cycles of CLK_I between successive CHS_O_STRB's. After the controller strobes for the first data word, EPR will transition low when the AMBE-1000™ responds to the interrupt. Once EPR is low the AMBE-1000™ will send out 16 more data words to the channel interface, to make up a complete frame packet.

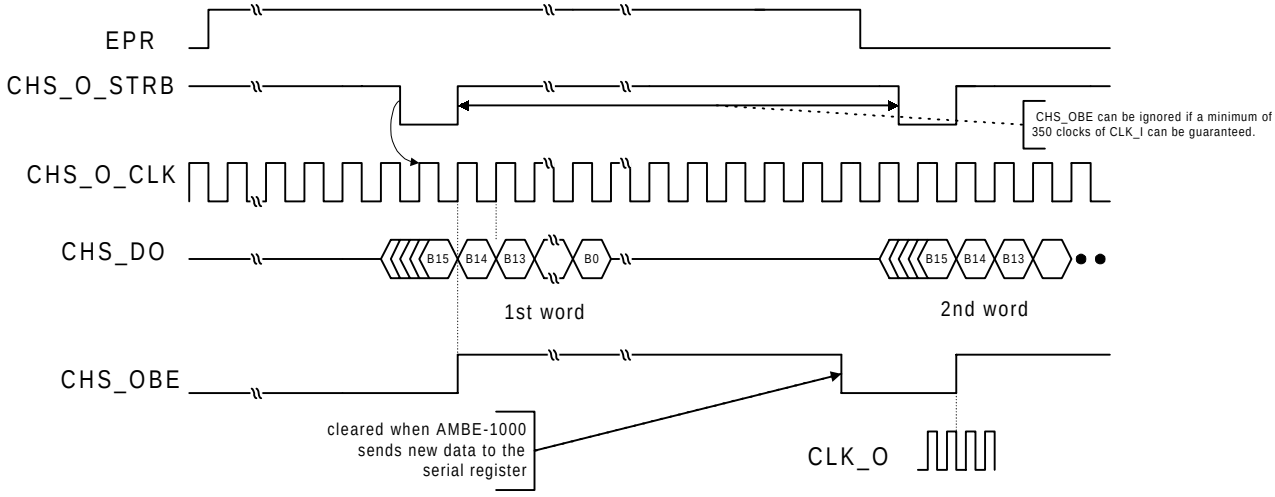


Figure 3.2.3-1 Encoder Passive mode timing

3.2.4 Packetized Serial Active Mode

In order to operate the AMBE-1000™ channel serial port in the active mode, the AMBE-1000™ pin configuration shown in figure 3.2.4-1 **MUST** be implemented.

The timing for active Packetized Serial mode is shown in figure 3.2.4-2. In this mode the AMBE-1000™ is in control of the channel interface. As shown in the timing diagram, when CHS_SYNC transitions low the AMBE-1000™ will begin to **transmit encoded data** and **receive decoder data**.

CHS_SYNC stays low for 64 CHS_O_CLK cycles and high for 64 CHS_O_CLK cycles. Also in this mode of operation, the frequency of CHS_O_CLK is $\frac{CLK\_I}{6}$. Figure 3.2.4-3 shows the appropriate configuration of connecting two AMBE-1000™ together via the serial channel interface. Note that one AMBE-1000™ is configured in the active mode, while the other is in the passive mode.

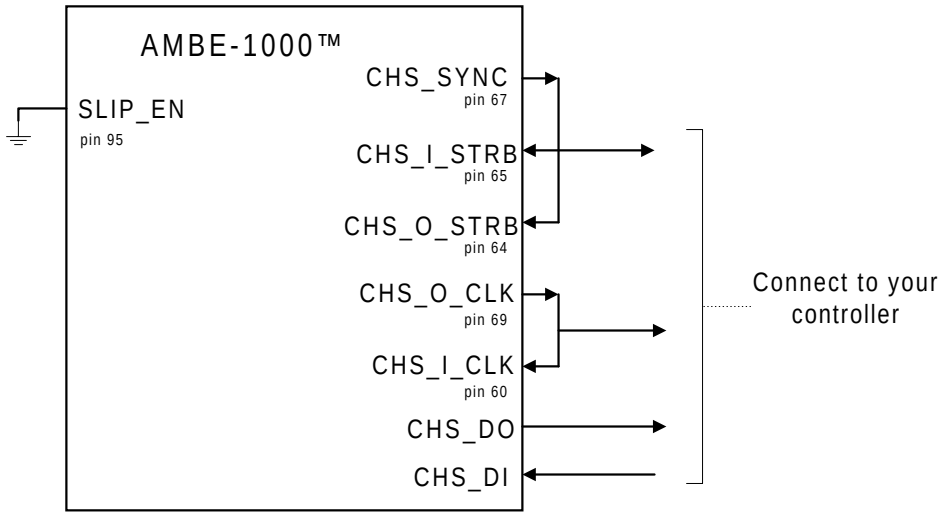


Figure 3.2.4-1 AMBE-1000™ Channel Serial port Active setting

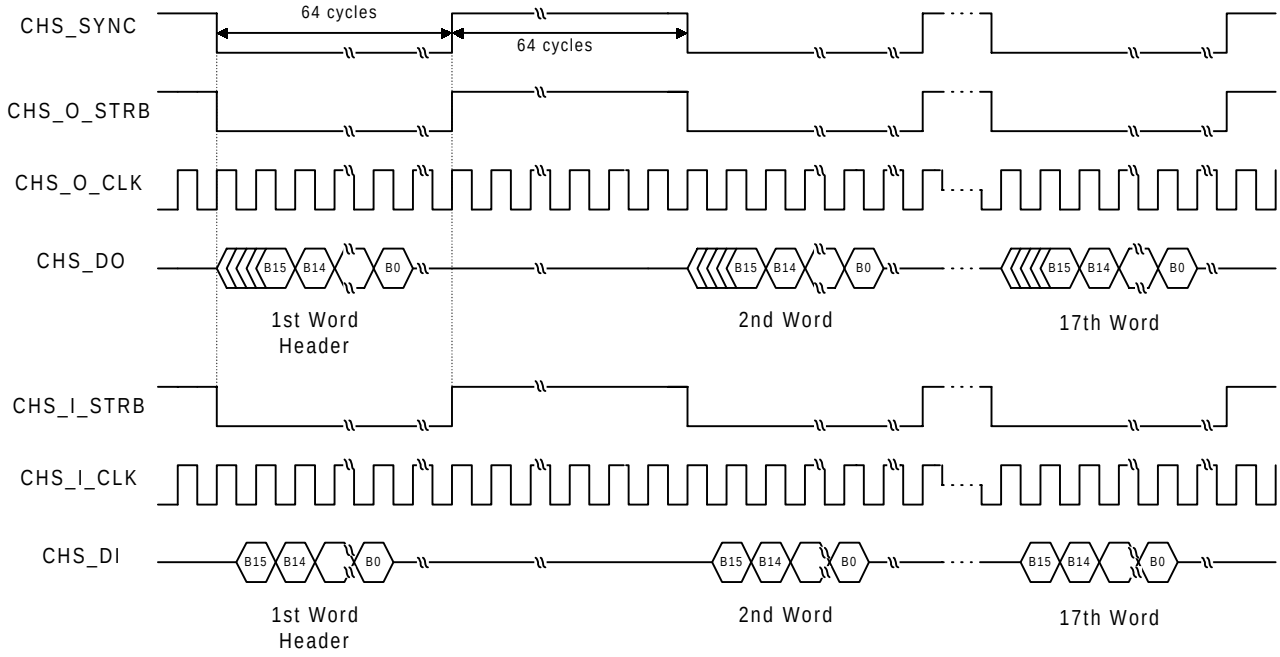


Figure 3.2.4-2 Active Channel Serial mode timing

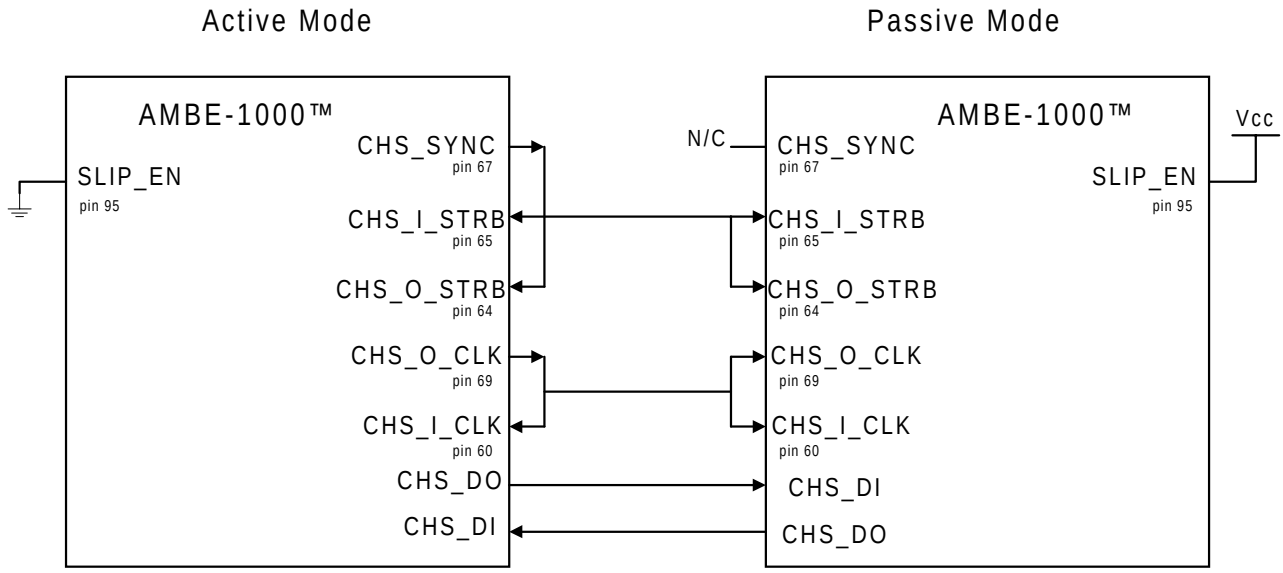


Figure 3.2.4-3 AMBE-1000™ connected together, one in active mode, the other in passive

The packetized serial data that is sent to and received from the AMBE-1000™ has the same format that was shown in figure 3.1.1-1 and is shown again in figure 3.2.1-5 for convenience.

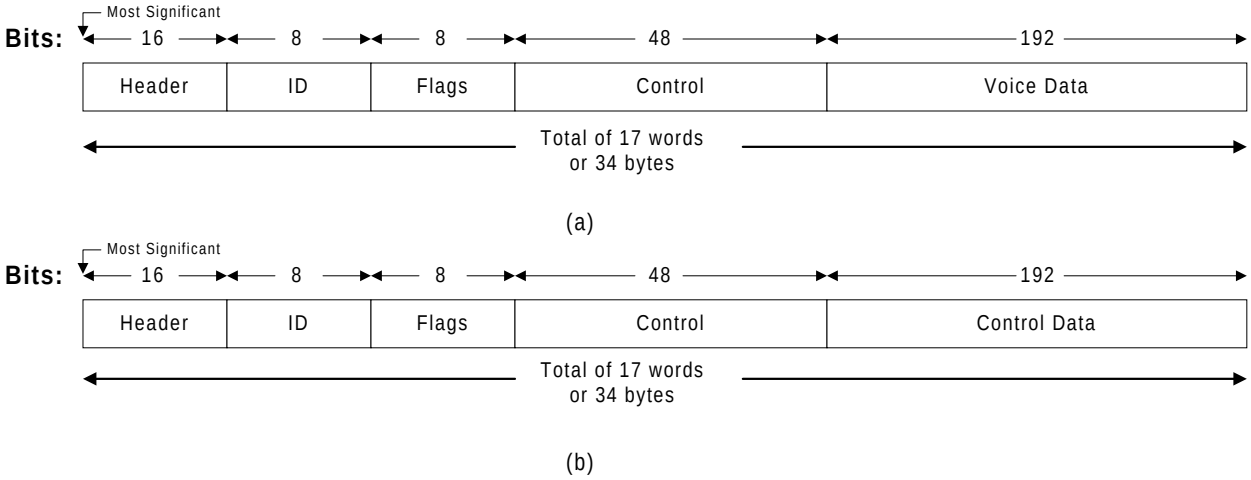


Figure 3.2.1-5 Packet Format

All the bit definitions that were discussed in the parallel interface section (section 3.1) will apply here.

3.2.5 Unformatted Serial

This mode may be used when there is no host processor or controller in the system. The proper pin configuration must be set in order to receive data in this mode. Table 3.2.2-1 is an abbreviated version of that table showing only the pin configurations for the unformatted mode.

CH_SEL2	CH_SEL1	CH_SEL0	Interface type	Passive / Active
1	0	0	Serial	Unformatted Serial (self Sync on) 1 bit per baud CHS_I_CLK and CHS_O_CLK *Passive*
1	0	1		Unformatted Serial (self Sync on) 2 bits per baud CHS_I_CLK and CHS_O_CLK *Passive*
1	1	0		Unformatted Serial (self Sync on) 3 bits per baud CHS_I_CLK and CHS_O_CLK *Passive*
1	1	1		Unformatted Serial (self Sync on) 4 bits per baud CHS_I_CLK and CHS_O_CLK *Passive*

Note: CHS_I_CLK: Input Clock
CHS_O_CLK: Output Clock

Table 3.2.2-1 Pin selection for Unformatted serial data mode

3.2.5.1 Sending and receiving data

As the above table shows, there are four different baud rates that can be used with the AMBE-1000™. Each of the baud rates refers to the data part of the word sent over the channel. Figure 3.2.5.1-1 shows the word configuration of the unformatted serial data mode. The upper 4 bits (bits 15 - 12) contains the data information, the next four bits are control bits that determine the type of data being transmitted, and the last 8 bits are control data information. In this configuration there are essentially two clocks. One is the baud clock (CHS_I_STRB and CHS_O_STRB) and the other is the bit clock (CHS_I_CLK, CHS_O_CLK). As in packetized mode of operation, CHS_I_CLK, CHS_O_CLK must be synchronous to CHS_I_STRB and CHS_O_STRB. The timing diagram is shown in figure 3.2.5.1-2.

When data is being transmitted, the upper 3 *control* bits **MUST** be zero, otherwise the data from the channel is assumed to be control information (control words sent to the AMBE-1000™ will be discussed later). Figure 3.2.2.1-3 shows the format of the data word and a baud rate description.

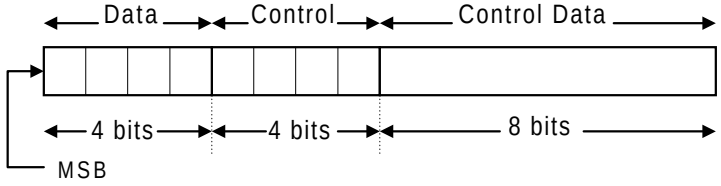


Figure 3.2.5.1-1 Unformatted word format

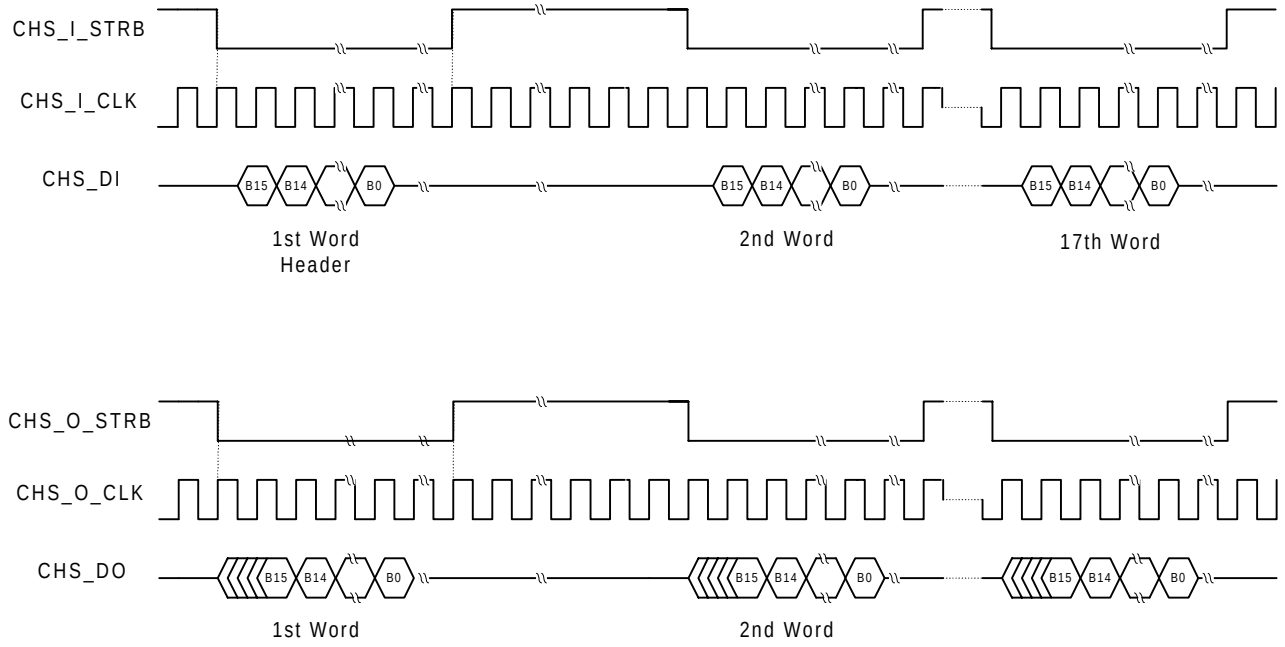


Figure 3.2.5.1-2 Timing diagram for the Unformatted serial data mode

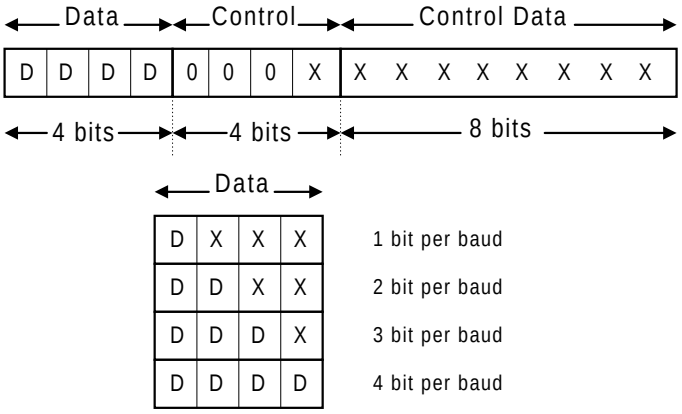


Figure 3.2.5.1-3 Unformatted serial data - data only

As an example of the AMBE-1000™ baud rate capabilities, if the baud clock is 2400 Hz (CHS_I_STRB, CHS_O_STB) then, the AMBE-1000™ can operate in 1 bit per baud for 2400 bps, 2 bits per baud for 4800 bps, 3 bits per baud for 7200 bps, or 4 bits per baud for 9600 bps. The maximum date rate for the AMBE-1000™ is 9600 bps, therefore, if the baud clock is 9600 Hz, the AMBE-1000™ is restricted to operate at one bit per baud.

The first bit of every 20 millisecond frame will be an alternating 0, 1 pattern which will be used for synchronization. Therefore, if the AMBE-1000™ is programmed to send/receive data at 2400 bps,

the first bit of the 48 bits per frame sent to/from the channel will be a synchronization bit. The synchronization process can take a minimum of 15 frames (~300 milliseconds) to complete.

3.2.5.2 Unformatted Control Information

This mode is similar to the packetized version of sending control information to the AMBE-1000™ except for a few minor details. They are as follows:

1. No header is required in this mode.
2. Control words 1 2 and 3 of the Packetized Mode's format are not required. (unless this particular packet is changing the data rate. See Table 3.1.1.2-3 for an example of the packetized format)

In this mode, the control bits are used as an offset inside the AMBE-1000™ and you are required to start with the control bits equal to 0x02. Since the AMBE-1000™ reads the control information in words, the same offset is repeated twice to create a word of information. All ID's , flags, control information, and A/D-D/A configuration packets are the same as the packetized mode except that the information will be transferred in bytes, in the control data part of the word. Table 3.2.2.2-1 shows some example control packets that can be sent to the AMBE-1000™. The lower 8 bits of each word in Table 3.2.2.2-1 are similar to packets shown in previous sections.

Please note that there is **NO HEADER required** in this format. Also please note that in this mode a maximum of 13 words (26 bytes) can be sent to the AMBE-1000™. After the 26 bytes(or 13 words) is sent to the AMBE-1000™, 0x0f00 (end of packet word) must be sent. It is possible to OVERWRITE control information, before the 0x0f00 word is sent, by re-sending the two words with the same offset number before the end of packet word is sent. See table 3.2.2.2-1 for an example of this procedure.

	Control Packets			
	Wake-Up	**CSP1027 A/D-D/A control packet**	**Control Packet to change data rate**	**Example packet with overwriting some data before end of packet is sent**
Control 1 / ID	0x02fe	0x0203	0x0201	0x0201
Control 2 / Flags	0x0280	0x0280	0x0200	0x0200
Control 3	0x0300	0x0303	0x03a3	0x0355
Control 4	0x0300	0x03c8	0x03c0	0x03c0
Control 5	0x0400	0x0480	0x04f2	0x0455
Control 6	0x0400	0x0400	0x0400	0x04c0
Control 7	0x0500	0x05ff	0x0500	0x050e
Control 8	0x0500	0x05fd	0x0500	0x0514
*	0x0600	0x061e	0x061e	0x060f
*	0x0600	0x06c0	0x06c0	0x065c
*	0x0700	0x0740	0x0740	0x0700
*	0x0700	0x0720	0x0720	0x0700
	0x0800	0x0880	0x0880	0x0800
	0x0800	0x080f	0x080f	0x0800
	0x0900	0x09d0	0x09d0	0x0900
	0x0900	0x0900	0x0900	0x0900
	0x0a00	0x0a00	0x0a00	0x0a00
	0x0a00	0x0a00	0x0a00	0x0a00
	0x0b00	0x0b00	0x0b00	0x0b00
	0x0b00	0x0b00	0x0b00	0x0b00
	0x0c00	0x0c00	0x0c00	0x0c00
	0x0c00	0x0c00	0x0c00	0x0c00
	0x0d00	0x0d00	0x0d00	0x0d00
	0x0d00	0x0d00	0x0d00	0x0d00
	0x0e00	0x0e00	0x0e00	0x0e00
	0x0e00	0x0e00	0x0e00	0x0e00
	0x0f00	0x0f00	0x0f00	0x0511
				0x051c
				0x061e
				0x062d
				0x0f00

Table 3.2.2.2-1 Control packet descriptions for unformatted serial data mode

4. Echo Canceller

The echo canceller can be activated in the AMBE-1000™ default configuration by enabling (=1) pin 92, ECHOCAN_EN.

The AMBE-1000™ voice encoder contains an echo canceller that can be selectively enabled or disabled in Control 5 (AMBE-1000™ word 1) of ID packet type **0x03**. The echo canceller can be enabled by setting the echo canceller flag (see section 3.1.1.4) to its active state (active=1).

The vocoder has a 5 millisecond echo canceller that is suitable for canceling the local echo caused by a 2-to-4 wire hybrid.

4.1 Echo Canceller Application Notes

The AMBE-1000™ contains a 5 millisecond echo canceller that is suitable for cancelling the local echo caused by a 2-to-4 wire hybrid and can achieve echo cancellation of approximately 30dB or more. Only the linear portion of the echo can be cancelled, so circuits should be designed to minimize non-linearities. The Echo Return Loss (ERL) of the analog circuit must be 6dB or more for proper echo canceller operation. Linear CODECs will generally provide better performance than mu-law or A-law CODECs due to lower quantization noise.

The AMBE-1000™ echo canceller sends a training sequence to the CODEC following a reset; the analog circuit causing the echo should be stable at this time. If the analog circuit causing the echo changes substantially, the echo canceller must be re-initialized, by resetting the AMBE-1000™ for optimum performance.

5. Voice Activation and Detection (VAD)

5.1 Voice Activation Enabled

VAD can be activated in the AMBE-1000™ default configuration by enabling (=1) pin 91, VAD_EN.

The AMBE-1000™ voice encoder contains a voice activation detection (VAD) algorithm that can be enabled or disabled in Control 5 (AMBE-1000™ word 1) of ID packet type **0x03**. VAD can be enabled by setting the VAD flag (see section 3.1.1.4) to it's active state (active=1).

5.2 Voice Activation Disabled

When disabled, the **Encoder Silence flag** in the flag area of the frame packet will always be inactive (=0).

5.3 Comfort Noise Insertion

The voice decoder supports voice activation by performing comfort noise insertion (CNI). When voice activation is enabled in the encoder, the corresponding decoder generates comfort noise during the period when the encoder has detected silence or background noise.

6. Dual Tone Multiple Frequency (DTMF)

The AMBE-1000™ is capable of detecting, transmitting, and re-generating DTMF tones. When the encoder detects DTMF tones, the output packet will have its DTMF flag enabled (=1), a special DTMF ID word will appear in control word 2, and the Voice Data field will contain the DTMF tone data. When this Voice Data is received by an AMBE-1000™ decoder, it will regenerate the inband

tone. The AMBE-1000™ can also generate “Dual Tones” at many different frequencies. These features will be explained in the following paragraphs. DTMF is always enabled.

When the encoder detects a DTMF tone, a packet with an ID of 0x00 with the DTMF flag set will be sent. In this packet control word 2 will have the DTMF tone that was detected. Figure 6-1 shows the bit configuration for the DTMF tones. Table 6-1 shows the mapping of the DTMF codes to the DTMF digits. The amplitude part of the word is linear and should range from 0 to 255. The AMBE-1000™ is sending the DTMF word as a way for a controller to quickly determine that a DTMF tone was sent.

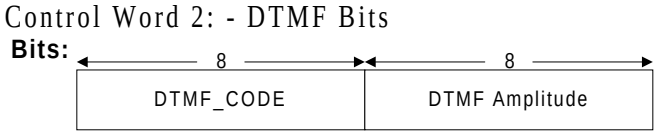


Figure 6-1 DTMF bits

DTMF Digit	DTMF CODE
1	0x00
2	0x04
3	0x08
4	0x01
5	0x05
6	0x09
7	0x02
8	0x06
9	0x0a
0	0x07
*	0x03
#	0x0b
A	0x0c
B	0x0d
C	0x0e
D	0x0f

Table 6-1 AMBE-1000™ DTMF codes

The AMBE-1000™ can also generate Dual Tones. This can be done by sending the AMBE-1000™ a data packet with an ID of 0x06 and setting the data to a specific pattern for each DTMF digit shown in Table 6-2. Table 6-2 is an example of the tones that can be generated by the AMBE-1000™. Contact DVSI for other tones that are not listed in the table.

	DTMF Digits						
	1	2	3	4	5	6	7
Header	0x13ec	0x13ec	0x13ec	0x13ec	0x13ec	0x13ec	0x13ec
ID/Flags	0x0600	0x0600	0x0600	0x0600	0x0600	0x0600	0x0600
Control 1	0x55c0	0x55c0	0x55c0	0x55c0	0x55c0	0x55c0	0x55c0
Control 2	0x55c0	0x55c0	0x55c0	0x55c0	0x55c0	0x55c0	0x55c0
Control 3	0x26d0	0x2ac0	0x2f43	0x26d0	0x2ac0	0x2f43	0x26d0
Control 4	0x164d	0x164d	0x164d	0x18a3	0x18a3	0x18a3	0x1b43
Control 5	0x0000	0x0000	0x0000	0x0000	0x0000	0x0000	0x0000
Control 6	0x0000	0x0000	0x0000	0x0000	0x0000	0x0000	0x0000
Control 7	0x0000	0x0000	0x0000	0x0000	0x0000	0x0000	0x0000
Control 8	0x0000	0x0000	0x0000	0x0000	0x0000	0x0000	0x0000
Control 9	0x0000	0x0000	0x0000	0x0000	0x0000	0x0000	0x0000
Control 10	0x0000	0x0000	0x0000	0x0000	0x0000	0x0000	0x0000
Control 11	0x0000	0x0000	0x0000	0x0000	0x0000	0x0000	0x0000
Control 12	0x0000	0x0000	0x0000	0x0000	0x0000	0x0000	0x0000
Control 13	0x0000	0x0000	0x0000	0x0000	0x0000	0x0000	0x0000
Control 14	0x0000	0x0000	0x0000	0x0000	0x0000	0x0000	0x0000
Control 15	0x0000	0x0000	0x0000	0x0000	0x0000	0x0000	0x0000

Table 6-2 Packet descriptions to generate DTMF tones

	DTMF Digits						
	8	9	0	Dial Tone	Busy	Ring	Silence
Header	0x13ec	0x13ec	0x13ec	0x13ec	0x13ec	0x13ec	0x13ec
ID/Flags	0x0600	0x0600	0x0600	0x0600	0x0600	0x0600	0x0600
Control 1	0x55c0	0x55c0	0x55c0	0x55c0	0x55c0	0x55c0	0xd800
Control 2	0x55c0	0x55c0	0x55c0	0x55c0	0x55c0	0x55c0	0xd800
Control 3	0x2ac0	0x2f43	0x2ac0	0x0b33	0x0f5c	0x0e14	0x0e14
Control 4	0x1b43	0x1b43	0x1e1c	0x0e14	0x13d7	0x0f5c	0x0f5c
Control 5	0x0000	0x0000	0x0000	0x0000	0x0000	0x0000	0x0000
Control 6	0x0000	0x0000	0x0000	0x0000	0x0000	0x0000	0x0000
Control 7	0x0000	0x0000	0x0000	0x0000	0x0000	0x0000	0x0000
Control 8	0x0000	0x0000	0x0000	0x0000	0x0000	0x0000	0x0000
Control 9	0x0000	0x0000	0x0000	0x0000	0x0000	0x0000	0x0000
Control 10	0x0000	0x0000	0x0000	0x0000	0x0000	0x0000	0x0000
Control 11	0x0000	0x0000	0x0000	0x0000	0x0000	0x0000	0x0000
Control 12	0x0000	0x0000	0x0000	0x0000	0x0000	0x0000	0x0000
Control 13	0x0000	0x0000	0x0000	0x0000	0x0000	0x0000	0x0000
Control 14	0x0000	0x0000	0x0000	0x0000	0x0000	0x0000	0x0000
Control 15	0x0000	0x0000	0x0000	0x0000	0x0000	0x0000	0x0000

Table 6-2 (continued)

Each tone packet generates 20 milliseconds of output tones. The length of the output tones can be extended by repeating the tone packet.

7. Low Power Modes

The AMBE-1000™ can be placed into a low power mode by either hardware or software. The AMBE-1000™ supports 2 Hardware and 4 Software low power modes

The AMBE-1000™ can be placed into a low-power or stand-by mode by sending the proper ID and control information in the frame packet.

The AMBE-1000™ has four different low power states that can be entered, but it should be noted that no voice data will be processed when those commands are issued in a frame. Once the command is received, the vocoder will then begin powering down into a power savings stand-by mode or sleep state. In this mode the vocoder will "wake-up" when it receives a channel interrupt (serial or parallel) or RESETN is asserted. The type of "wake-up" needed will depend on the type of lower power mode the AMBE-1000™ is in. This will be explained in the next few paragraphs. *It should be noted that in all low power modes the A/D-D/A port will be disabled.*

The hardware low power mode is enabled (=0) by placing the H_STOPN pin to low, once enabled the only way to return to normal processing mode is by placing the AMBE-1000™ into reset. The wake-up latency of this method is approximately 200 microseconds at reset. The AMBE-1000™ can also be placed into Standard Sleep mode by enabling (=1) SLEEP_EN. As discussed in section 3.1.1.3, a packet of ID type **0xFE MUST** be sent to return to normal processing mode.

The different low power modes that the AMBE-1000™ supports with the modes typical power dissipation is shown in Table 7-1

Mode	Clock type	Power Consumption		Wake up Latency
		5V	3V	
Standard Sleep	crystal	66 mW	24 mW	3T*
	CMOS, TTL	36 mW	13 mW	3T*
Slow Clock Sleep	crystal	33 mW	11.0 mW	from reset approx. 200 μS
	CMOS, TTL	3 mW	0.6 mW	|
Slow Clock Sleep with disabled crystal oscillator	crystal	1.2 mW	0.31 mW	| |
Software Stop	crystal	0.55 mW	0.11 mW	|
	CMOS, TTL	0.55 mW	0.11 mW	|
Hardware Stop	crystal	30 mW	10.7 mW	|
	CMOS, TTL	0.55 mW	0.11 mW	↓

*T = CLK_I clock cycle.

Table 7-1 Low power mode power dissipation

The following packets shown in Table 7.2 must be sent to the AMBE-1000™ in order to enter the proper low power mode by software command packet. Please remember that a frame packet is **17**

words (34 bytes) in length and the information shown in Table 7-2 is only control information needed . The user must pad the packets so that the number of words sent to the AMBE-1000™ is 17.

	Standard Sleep	Slow Clock Sleep	Slow Clock Sleep with crystal disabled	Software Stop
Header	0x13ec	0x13ec	0x13ec	0x13ec
ID/Flag	0x0400	0x0400	0x0400	0x0400
Control 1	0x0000	0x0001	0x0001	0x0001
Control 2	0xXXXX	0x000c	0x000c	0x0000
Control 3	0xXXXX	0x0000	0x0000	0x4000
Control 4	0xXXXX	0x0000	0x40d0	0xd000
Control 5	0xXXXX	0x40d0	0xc0d0	0xf000
Control 6	0xXXXX	0x8000	0x8000	0x0000
Control 7	0xXXXX	0x00f0	0x40c0	0x4000
Control 8	0xXXXX	0x0000	0x2710	0x2710
Control 9	0xXXXX	0x0000	0x00d0	0x0000
Control 10	0xXXXX	0x0000	0x0000	0x0000
Control 11	0xXXXX	0x0000	0x0000	0x0000
Control 12	0xXXXX	0x0000	0x0000	0x0000
Control 13	0xXXXX	0x0000	0x0000	0x0000
Control 14	0xXXXX	0x0000	0x0000	0x0000
Control 15	0xXXXX	0x0000	0x0000	0x0000

Table 7.2 Low Power Command Packets

When the AMBE-1000™ is in the **slow clock sleep, slow clock sleep with crystal disabled, or software stop low power mode**, the vocoder will not respond to the channel or A/D-D/A interrupts. The only way to “wake-up” the vocoder is by asserting the RESETN pin.

If the AMBE-1000™ is in the standard sleep mode, the wake-up packet shown in Table 7-3 **MUST** be sent to the AMBE-1000™ so that it can resume normal processing.

	Wake-up
Header	0x13ec
ID/Flags	0xfe80
Control 1	0x0000
Control 2	0x0000
Control 3	0x0000
Control 4	0x0000
Control 5	0x0000
Control 6	0x0000
Control 7	0x0000
Control 8	0x0000
Control 9	0x0000
Control 10	0x0000
Control 11	0x0000
Control 12	0x0000
Control 13	0x0000
Control 14	0x0000
Control 15	0x0000

Table 7-3 Standard Sleep mode wake-up packet

7.1 Sleep Enable

SLEEP_EN (Pin 93) is tied high if you want the AMBE-1000™ to go directly into standard sleep mode upon power-up or reset. This will allow you to re-program your A/D-D/A chip and/or the AMBE-1000™ chip before you begin normal processing mode. Remember, the AMBE-1000™ does ***not*** have to be placed into standard sleep mode. The AMBE-1000™ can be re-programmed on-the-fly by sending the 0x01 ID packet with the new information. To re-program the A/D-D/A chip, the AMBE-1000™ ***must be placed into standard sleep mode***. This can be done by sending the appropriate packet (see previous section).

8. Scheduler (SLIP_EN)

In most real-time applications, the scheduler (**SLIP_EN**) should be enabled to account for any slip or synchronization delay between the AMBE-1000™ and the communication channel timing. The scheduler adjusts the timing of the AMBE-1000™ based on the controller's **EPR** response time (***EPR** response time* is the amount time it takes for the controller to respond to AMBE-1000™ **EPR** signal). Therefore, if the **EPR** response time varies because of the controller synchronization with the communications channel (this is the recommended mode of operation), **SLIP_EN** should be enabled. A Time division multiplexed (TDM) channel is an example of when **EPR** response can be delayed by the controller. The controller must wait for the appropriate time slot before it can send data to the channel. Figure 8-1 shows two AMBE-1000™s that are in passive mode with a TDM channel. Here both **SLIP_EN**'s are enabled because there is a TDM channel being used.

If the controller responds to an **EPR** almost immediately and takes the data from the AMBE-1000™ for *instantaneous* transfer to the channel, then **SLIP_EN** does not have to be enabled.

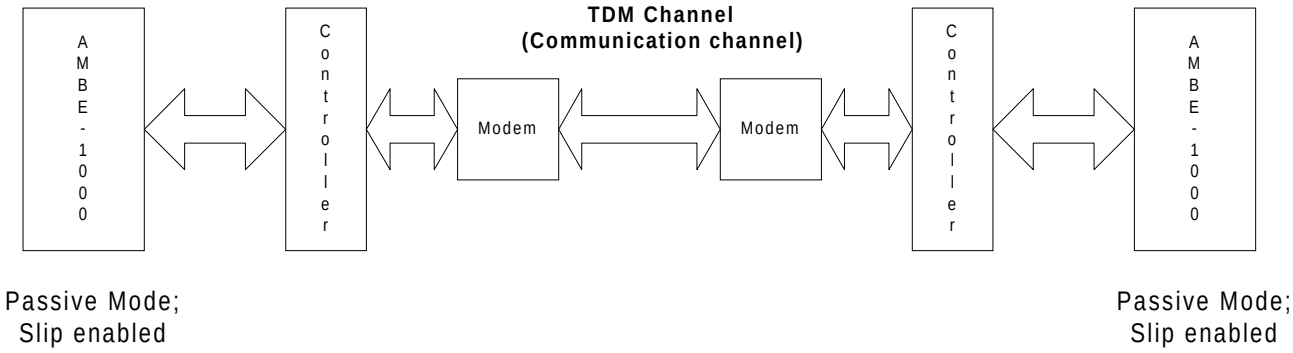


Figure 8-1 AMBE-1000™s with a TDM channel

Another example of when to enable **SLIP_EN** would be if ***EPR*** and ***DPE*** are not used to control the data into and out of the AMBE-1000™, but this will probably only occur if two AMBE-1000™'s are connected back-to-back. Figure 8-2 shows two AMBE-1000™s connect back-to-back, one in parallel active mode **SLIP_EN** disabled, the other in parallel passive mode with **SLIP_EN** enabled. It should be noted that in this configuration the **EPR and DPE** signals are not used.

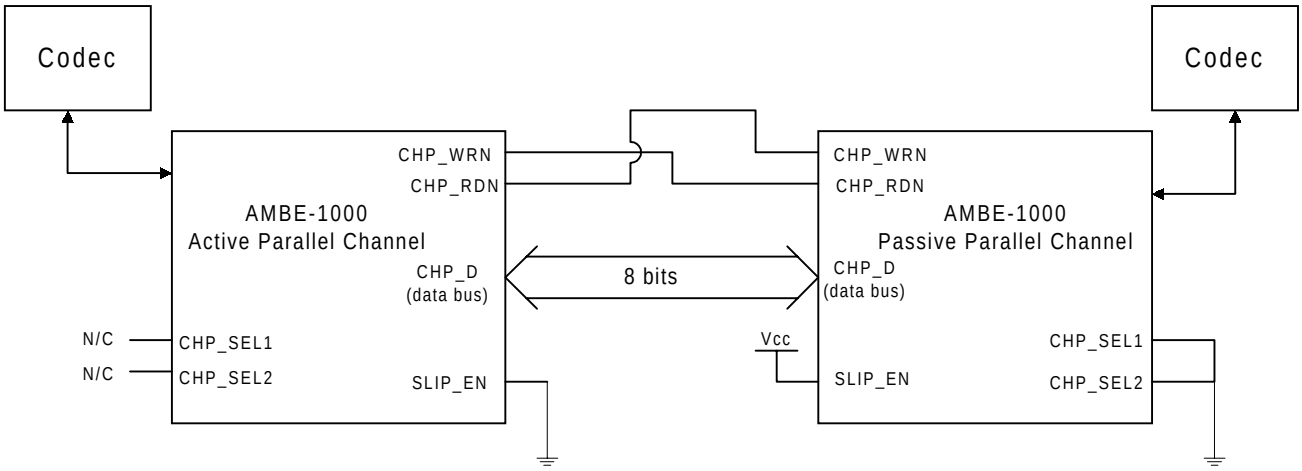


Figure 8-2 Connect two AMBE-1000™ through parallel channel interface

Figure 8-3 shows the serial channel interface with **SLIP_EN** is enabled. If **EPR** and **DPE** are not used for the timing of the passive mode channel interface then the SLIP_EN pin must be enabled.

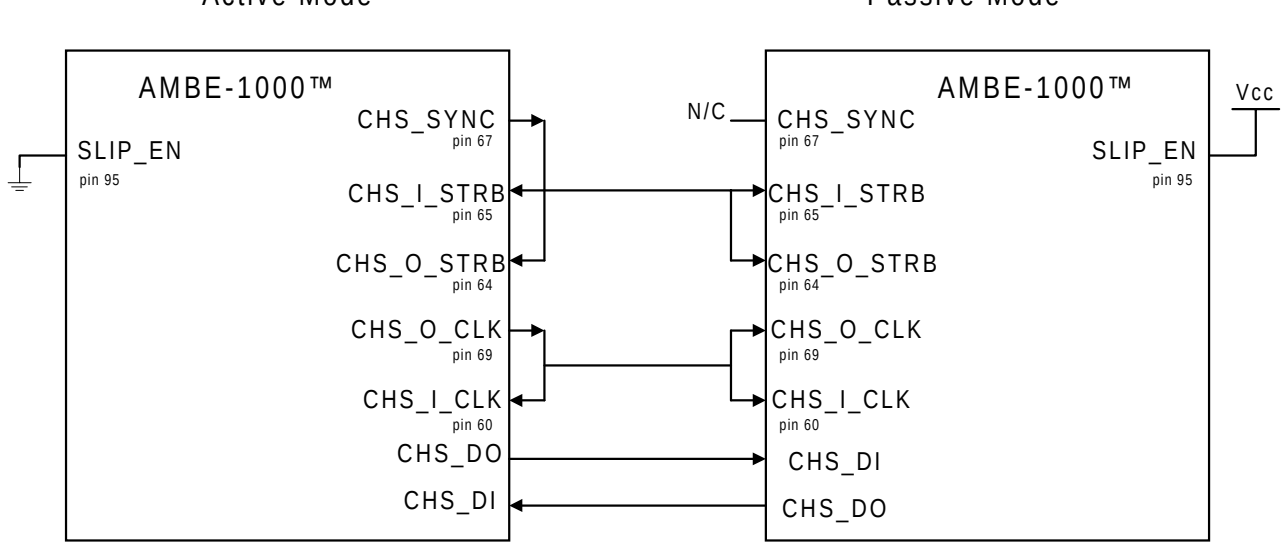


Figure 8-3 Connect two AMBE-1000™ through serial channel interface

9. License Information

Digital Voice Systems, Inc.
AMBE-1000™ END USER License Agreement

1.0 Preliminary Statements and Definitions

1.1 "END USER" shall mean the person and/or organization to whom the AMBE-1000 was delivered or provided to as specified in the purchase order or other documentation. In the event that the END USER transfers his rights under this license to a third party as specified in section 2.2, then this third party shall become an "END USER".

1.2 Digital Voice Systems, Inc. (DVSI) has developed a voice coding method and algorithm (the "Technology") based on the Advanced Multi-Band Excitation ("AMBE®") speech coder. The technology codes speech at bit rates of 2.4 to 9.6 kilobits per second (kbps) including error correction bits.

1.3 "AMBE® Software" shall mean the speech coding software and/or firmware integrated into the AMBE-1000™ integrated circuit.

1.4 "Voice Codec" shall mean the AMBE-1000™ integrated circuit, the AMBE® Software, firmware and associated documentation, including modifications, enhancements and extensions made by or for Digital Voice Systems, Inc. (DVSI) and including circuit diagrams, timing diagrams, logic diagrams, layouts, operating instructions and user manuals.

1.5 DVSI represents that it owns certain "Proprietary Rights" in the Technology and the AMBE® Software, including patent rights in the Technology, and patent rights, copyrights, and trade secrets in the AMBE® Software.

2.0 License Granted

2.1 Subject to the conditions herein and upon initial use of the AMBE-1000™ Voice Codec, DVSI hereby grants to END USER a non-exclusive, limited license to use the AMBE® Software in machine readable form solely on the AMBE-1000™ Voice Codec. Title to the AMBE® Software remains with DVSI. No license is granted for use of the AMBE® Software on other than the AMBE-1000™ Voice Codec. No license, right or interest in any trademark, trade name or service mark of DVSI is granted under this Agreement.

2.2 Transfer of License

The END USER shall have the right to transfer the AMBE-1000™ and all rights under this Agreement to a third party by either (i) providing the third party with a copy of this Agreement or (ii) providing the third party with an agreement written by the END USER (hereinafter "END USER Agreement") so long as the END USER Agreement is approved in writing by DVSI prior to transfer of the AMBE-1000™. The END USER Agreement shall contain comparable provisions to those contained herein for protecting the Proprietary Information from disclosure by such third party. Third parties shall agree to accept all the terms and conditions under either Agreement or the END USER Agreement.

2.3 END USER shall not copy, extract, de-compile, reverse engineer or disassemble the AMBE® Software contained in the AMBE-1000™.

3.0 Term and Termination

3.1 This Agreement is effective upon initial delivery of the Voice Codec and shall remain in effect until terminated in accordance with this agreement.

3.2 This Agreement shall terminate automatically without notice from DVSI if END USER fails to comply with any of the material terms and conditions herein. END USER may terminate this Agreement at any time upon written notice to DVSI certifying that END USER has complied with the provisions of Section 3.3.

3.3 Upon termination of this Agreement for any reason, END USER shall: (i) return all AMBE-1000™ voice codecs purchased or acquired, or in Licensee's possession, to DVSI; (ii) have no further rights to any AMBE® Software or the Technology without a separate written license from DVSI; (iii) discontinue all use of the AMBE-1000™;

4.0 Payments

4.1 In consideration of the materials provided as part of the Voice Codec, and in consideration of the license and rights in the AMBE® Software granted by DVSI, and in consideration of DVSI's performance of its obligations hereunder, END USER agrees to pay to DVSI the fee specified in DVSI's invoice.

5.0 Proprietary Notices

END USER shall not remove any copyright or proprietary notice on the AMBE-1000™ or on the AMBE® Software.

6.0 Proprietary Information

6.1 The parties agree that the AMBE® Software shall be considered Proprietary Information.

6.2 Except as otherwise provided in this Agreement, END USER shall not use, disclose, make, or have made any copies of the Proprietary Information, in whole or in part, without the prior written consent of DVSI.

7.0 Limited Warranty

7.1 DVSI warrants the Voice Codec to be free from defects in materials and workmanship under normal use for a period of ninety (90) days from the date of delivery.

7.2 Except as stated in Section 7.1, the Voice Codec is provided "as is" without warranty of any kind. DVSI does not warrant, guarantee or make any representations regarding the use, or the results of the use, of the Voice Codec with respect to its correctness, accuracy, reliability, currentness or otherwise. The entire risk as to the results and performance of the Voice Codec is assumed by the END USER. After expiration of the warranty period, END USER, and not DVSI or its employees, assumes the entire cost of any servicing, repair, replacement, or correction of the Voice Codec.

7.3 DVSI represents that, to the best of its knowledge, it has the right to enter into this Agreement and to grant a license to use the AMBE® Software to END USER.

7.4 Except as specifically set forth in this Section 7.0, DVSI makes no express or implied warranties including, without limitation, the warranties of merchantability or fitness for a particular purpose or arising from a course of dealing, usage or trade practice, with respect to the Voice Codec. Some states do not allow the exclusion of implied warranties, so the above exclusion may not apply to END USER. No oral or written information or advice given by DVSI or its employees shall create a warranty or in any way increase the scope of this warranty, and END USER may not rely on any such information or advice. The limited warranties under this section 7.0 give END USER specific legal rights, and END USER may have other rights which vary from state to state.

8.0 Limitation of Liability

8.1 In no event shall DVSI be liable for any special, incidental, indirect or consequential damages resulting from the use or performance of the Voice Codec whether based on an action in contract, tort (including negligence) or otherwise (including, without limitation, damages for loss of business profits, business interruption, and loss of business information), even if DVSI or any DVSI representative has been advised of the possibility of such damages.

Because some states do not allow the exclusion or limitation of liability for consequential or incidental damages, the above limitations may not apply to END USER.

8.2 DVSI's maximum liability for damages arising under this Agreement shall be limited to 20% (twenty percent) of the fees paid by END USER for the particular Voice Codec which caused the damages or that is the subject matter of, or is directly related to, the cause of action.

9.0 Taxes

All payments required under Section 4.0 or otherwise under this Agreement are exclusive of taxes and END USER agrees to bear and be responsible for the payment of all such taxes (except for taxes based upon DVSI's income) including, but not limited to, all sales, use, rental receipt, personal property or other taxes which may be levied or assessed in connection with this Agreement.

10.0 Export

United States export laws and regulations prohibit the exportation of certain products or technical data received from DVSI under this Agreement to certain countries except under a special validated license. As of May 20, 1996 the restricted countries are: Libya, Cuba, North Korea, Iraq, Serbia, Montenegro, and Iran. The END USER hereby gives its assurance to DVSI that it will not knowingly, unless prior authorization is obtained from the appropriate U.S. export authority, export or re-export, directly or indirectly to any of the restricted countries any products or technical data received from DVSI under this Agreement in violation of said United States Export Laws and Regulations. DVSI neither represents that a license is not required nor that, if required, it will be issued by the U.S. Department of Commerce. Licensee shall assume complete and sole responsibility for obtaining any licenses required for export purposes.

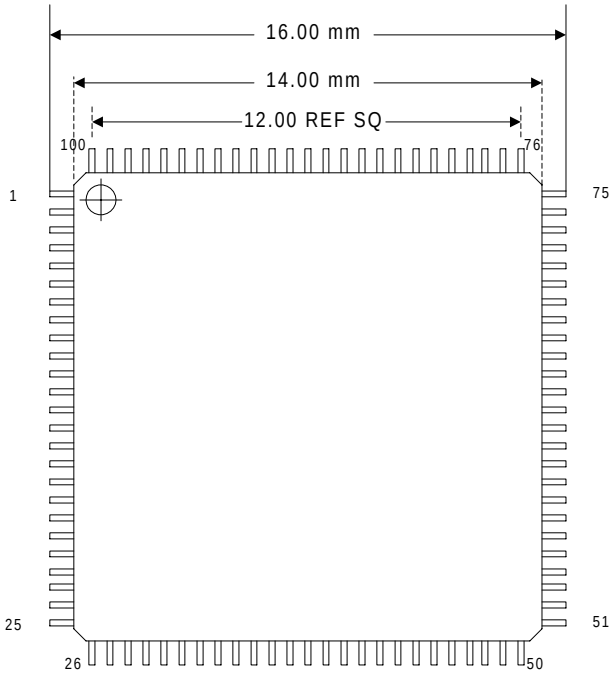
11.0 Governing Law

This Agreement is made under and shall be governed by and construed in accordance with the laws of the Commonwealth of Massachusetts, except that body of law governing conflicts of law. If any provision of this Agreement shall be held unenforceable by a court of competent jurisdiction, that provision shall be enforced to the maximum extent permissible, and the remaining provisions of this Agreement shall remain in full force and effect.

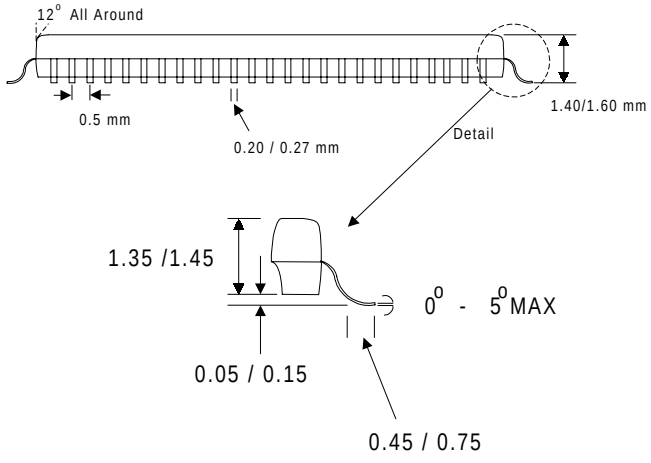
1. Appendix

1.1 Package Description

100 pin TQFP (Thin Quad Flat Pack)
All Dimensions are in millimeters



Not Drawn to Scale



1.2 Pin Information

Pin Information

Pin Number	Pin Name	Pin Type	Parallel Mode	Serial Mode	Description
1	GND				
2	CH_SEL0	I	I	I	Channel Interface Select bit 0
3	BPS_SEL3	I	I	I	Default Bit Rate select bit3
4	BPS_SEL2	I	I	I	Default Bit Rate select bit2
5	BPS_SEL1	I	I	I	Default Bit Rate select bit1
6	BPS_SEL0	I	I	I	Default Bit Rate select bit0
7	VDD				
8	N/C				
9	N/C				
10	N/C				
11	N/C				
12	N/C				
13	GND				
14	N/C				
15	GND				
16	N/C				
17	N/C				
18	N/C				
19	VDD				
20	N/C				
21	N/C				
22	N/C				
23	N/C				
24	N/C				
25	GND				
26	VDD				
27	N/C				
28	N/C				
29	N/C				
30	N/C				
31	N/C				
32	GND				
33	N/C				
34	N/C				
35	N/C				
36	N/C				
37	CLK_I	I	I	I	
38	CLK_I2	I	I	I	
39	RESETN	I	I	I	Reset (Active low / Inactive High)
40	CLK_O	O	O	O	Processor clock output
41	GND				
42	N/C				

Pin Number	Pin Name	Pin Type	Parallel Mode	Serial Mode	Description
43	INT_0	N/C	N/C	N/C	Active High / Inactive Low
44	GND				
45	RESERVED - N/C				
46	EPR	O	O	O	Encoder Packet Ready
47	DPE	O	O	O	Decoder Packet Empty
48	N/C				
49	N/C				
50	VDD				
51	GND				
52	CHP_D7	O	O	N/C	Channel serial interface - N/C or Channel parallel interface bit 7
53	CHP_D6	O	O	N/C	Channel serial interface - N/C or Channel parallel interface bit 6
54	CHP_D5	O	O	N/C	Channel serial interface - N/C or Channel parallel interface bit 5
55	CHP_D4	O	O	N/C	Channel serial interface - N/C or Channel parallel interface bit 4
56	VDD				
57	CHP_D3	O	O	N/C	Channel serial interface - N/C or Channel parallel interface bit 3
58	CHP_D2	O	O	N/C	Channel serial interface - tied low or Channel parallel interface bit 2
59	CHS_DI CHP_D1	I	I	I	Channel serial interface Data input or Channel parallel interface bit 1
60	CHS_I_CLK CHP_D0	I	I	I	Channel serial interface input clock or Channel parallel interface bit 0
61	CHS_OBE CHP_OBE	O	O	O	Channel serial interface output buffer empty or Channel parallel interface output buffer empty
62	GND				
63	CHS_IBF CHP_IBF	O	O	O	Channel serial interface input buffer full or Channel parallel interface input buffer full
64	CHS_O_STRB CHP_RDN	I I/O	I/O	I/O	Channel serial interface output data strobe or Channel parallel interface output data strobe
65	CHS_I_STRB CHP_WRN	I I/O	I/O	I/O	Channel serial interface input data strobe or Channel parallel interface input data strobe
66	VDD				
67	CHS_SYNC N/C	O		O	Channel Serial interface sync bit or Channel parallel interface - no connect
68	CHS_DO	O		O	Channel serial interface data output or

Pin Number	Pin Name	Pin Type	Parallel Mode	Serial Mode	Description
68 (cont'd)	CHP_SEL1	I	Passive - GND Active - N/C		Channel parallel interface select 1
69	CHS_O_CLK CHP_SEL2	I/O I	 Passive - GND Active - N/C	I/O	Channel serial interface output clock or Channel parallel interface select 2
70	N/C				
71	N/C				
72	N/C				
73	GND				
74	CD_SADD	O	O	O	Serial Address (used for certain A/D-D/As)
75	GND				
76	H_STOPN	I	I	I	Active Low / Inactive High
77	N/C				
78	TX_DO	O	O	O	Data Output - (to A/D-D/A)
79	TX_STRB	I	I	I	A/D-D/A - Data Output Strobe
80	TX_O_CLK	I/O	I/O	I/O	A/D-D/A - Data Output Clock
81	RX_I_CLK	I	I	I	A/D-D/A - Data Input Clock
82	RX_STRB	I	I	I	A/D-D/A - Data Input Strobe
83	GND				
84	RX_DI	I	I	I	Data Input (from A/D-D/A)
85	VDD				
86	RX_IBF	O	O	O	Data Input buffer full
87	TX_OBE	O	O	O	Data output buffer empty
88	C_SEL0	I	I	I	A/D-D/A select bit 0
89	C_SEL1	I	I	I	A/D-D/A select bit 1
90	C_SEL2	I	I	I	A/D-D/A select bit 2
91	VAD_EN	I	I	I	Voice Activation and Detection Enable
92	ECHOCAN_EN	I	I	I	Echo Canceller Enable
93	SLEEP_EN	I	I	I	Standard Sleep Enable
94	GND				
95	SLIP_EN	I	I	I	Slip Enable
96	RESERVED - N/C				
97	RESERVED - N/C				
98	CH_SEL2	I	I	I	Channel Interface Select bit 2
99	CH_SEL1	I	I	I	Channel Interface Select bit 1
100	VDD				

1.3 Crystal / Oscillator

The AMBE-1000™ clock can has a frequency range of 26 - 30 MHz

If the option to use a crystal is chosen the following electrical characteristics and requirements apply.

To enable the crystal oscillator, connect the crystal across CLK_I and CLK_I2 along with one external capacitor from each of these pins to ground. Figure App1.3 shows a picture of this. DVSI recommends that C1 and C2 be 10 pF; but larger values may be necessary if precise frequency tolerance is required.

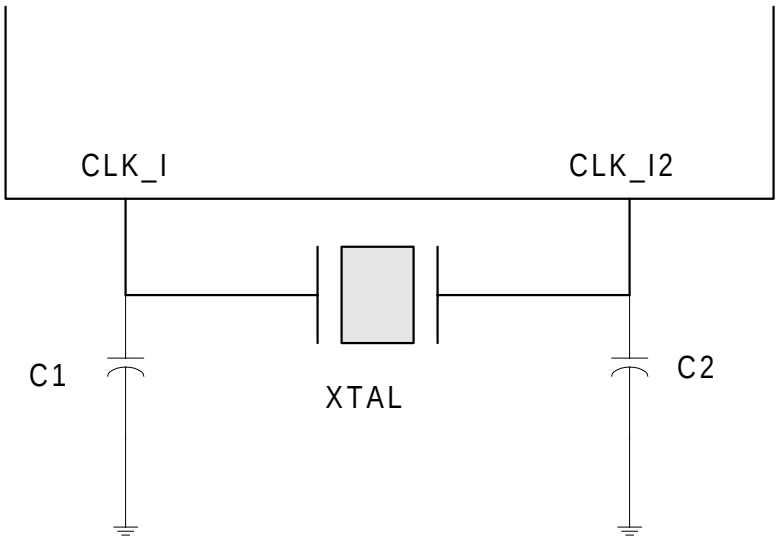


Figure App1.3

The following should be used as a guide when designing the printed circuit board layout.

- Keep the crystal and external capacitors as close to the CLK_I and CLK_I2 pins as possible to minimize board stray capacitance.
- Keep CLK_I and CLK_I2 away from high frequency digital traces (example CLK_O) to avoid coupling.

If you are supplying an external clock or oscillator, this signal should be connected to CLK_I and CLK_I2 must left open (N/C).

1.4 Electrical Characteristics and Requirements

Supply Voltage: 5 volts or 3.3 volts

Operating Temp: 40° C to +85°C

I/O Levels: CMOS

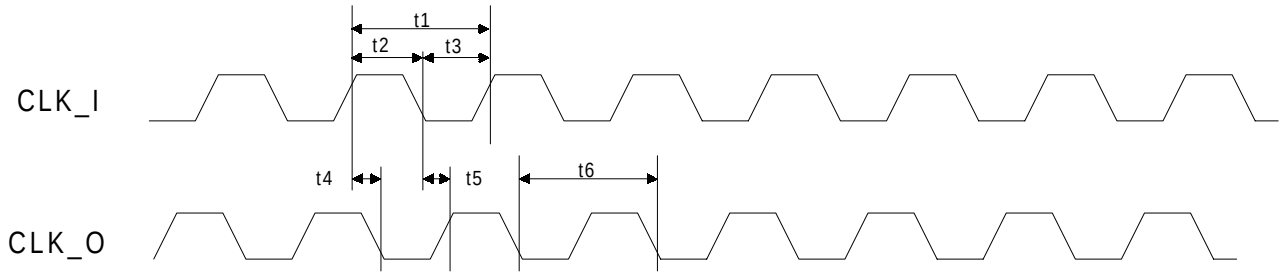
		Mode	Wake up Latency
Power:	~180mW @ 5 volts ~65mW @ 3.3 volts	Normal Processing	-
	36mW @ 5 volts 13mW @ 3.3 volts	Standard Sleep	3T*
	0.55mW @ 5 volts 0.11 mW @ 3.3 volts	Software Stop	from reset approx. 200 μS
	0.55mW @ 5 volts 0.11 mW @ 3.3 volts	Hardware Stop (CMOS, TTL)	| |
	3 mW @ 5 volts 0.6 mW @ 3.3 volts	Slow Clock (CMOS, TTL)	| |
	1.2 mW @ 5 volts 0.31 mW @ 3.3 volts	Slow Clock Sleep with disabled crystal oscillator	| ↓

* T = is one cycle of CLK_I.

1.5 Timing Information

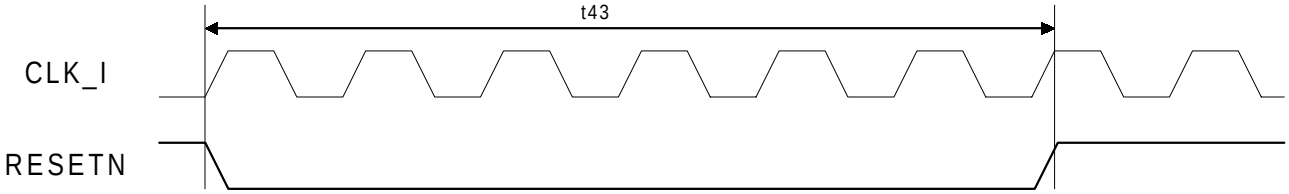
1.5.1 AMBE-1000™ Clock Generation

Timing Characteristics for the AMBE-1000™ clock generation.



Reference	Parameter			Units
		Min	Max	
t1	Clock Period (High to High)	30	-	ns
t2	Clock High Time (high to low)	12	-	ns
t3	Clock Low Time (low to high)	12	-	ns
t4	CLK_O Low Delay (high to low)	-	21	ns
t5	CLK_O High Delay	-	21	
t6	CLK_0 Period (low to low)	T*		

- T = t1

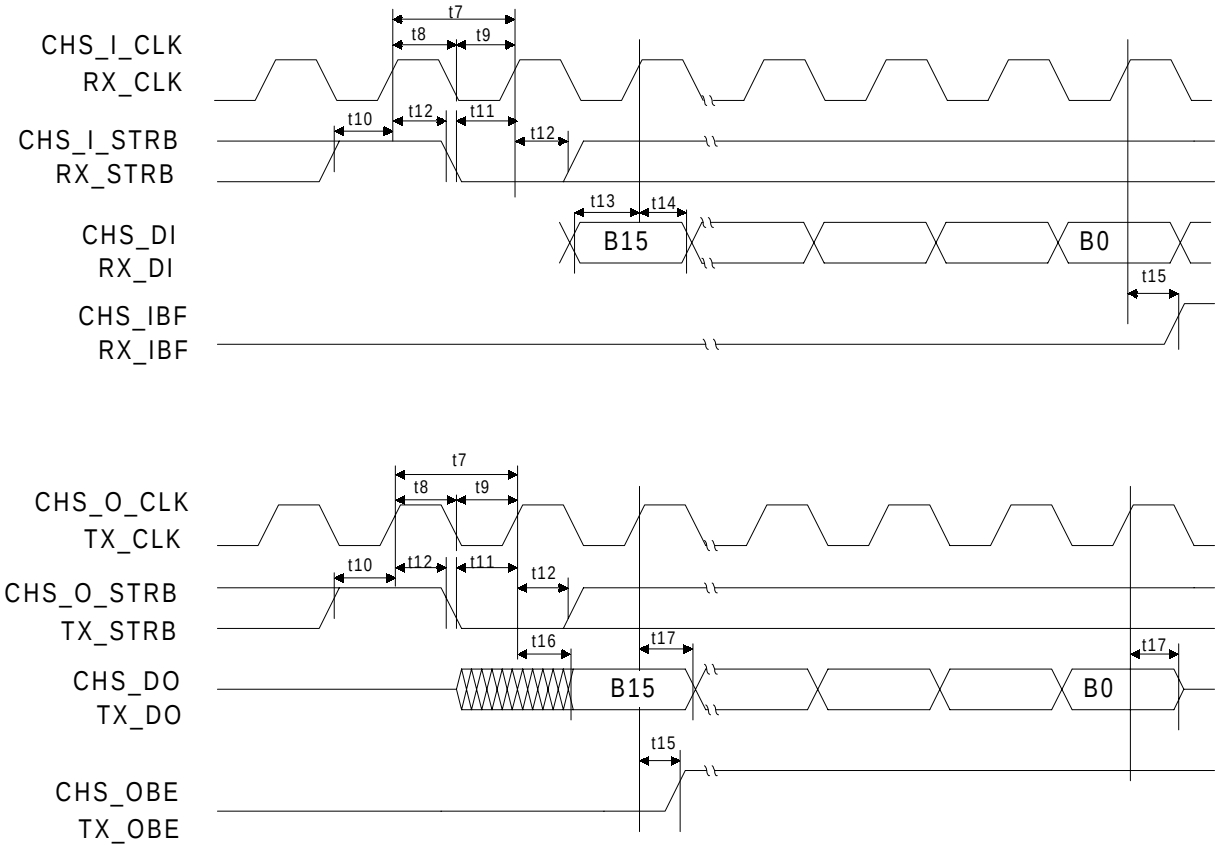


Reference	Parameter			Units
		Min	Max	
t43	Reset Timing	6T	-	ns

NOTE: The device needs to be clocked for at least six CLK_I cycles during reset after power-up. Otherwise, high currents may flow

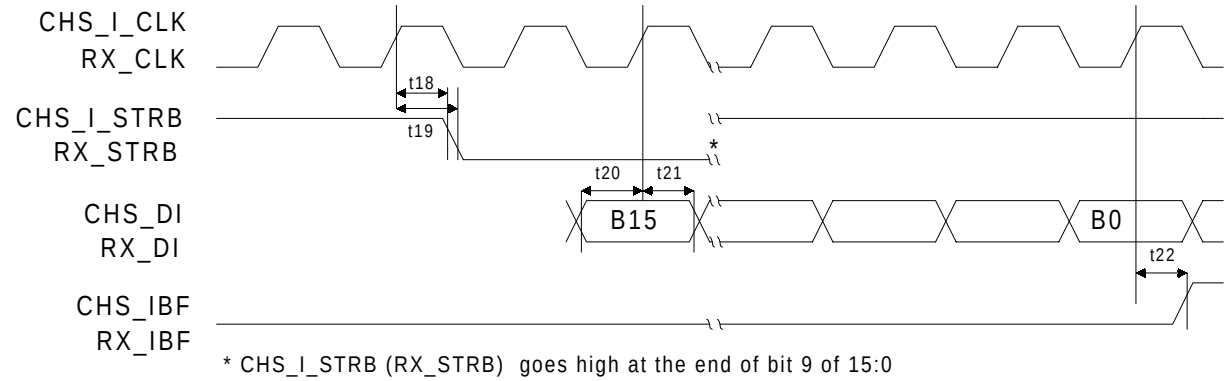
1.5.2 Channel Serial Port and A/D-D/A Port

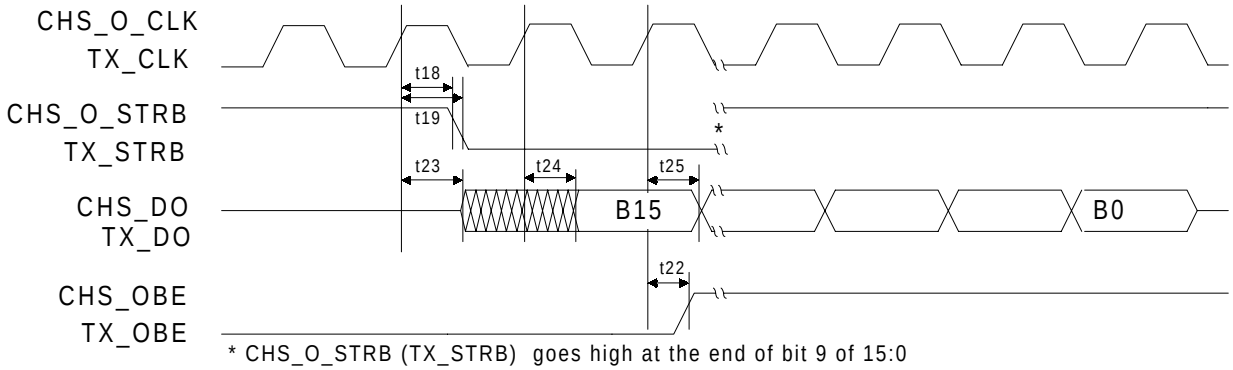
Timing Characteristics for Channel Serial Port Operation in Passive Packetized Mode or for the passive mode of the A/D-D/A port



Reference	Parameter	5 Volts		3 Volts		Units
		Min	Max	Min	Max	
t7	Clock Period (High to High)	60		66		ns
t8	Clock High Time (high to low)	27		30		ns
t9	Clock Low Time (low to high)	27		30		ns
t10	Load High Setup (high to high)	5		5		ns
t11	Load Low Setup (low to high)	5		5		ns
t12	Load High Hold (high to Invalid)	4		4		ns
t13	CHS_DI Setup (valid to high)	5		4		ns
t14	CHS_DI Hold (high to invalid)	4		5		ns
t15	CHS_IBF and CHS_OBE Delay		35		40	ns
t16	CHS_DO Delay (high to valid)		35		40	ns
t17	CHS_DO Hold (high to invalid)	5		15		ns

Timing Characteristics for Channel Serial Port Operation in Active Packetized Mode or for the active mode of the A/D-D/A port

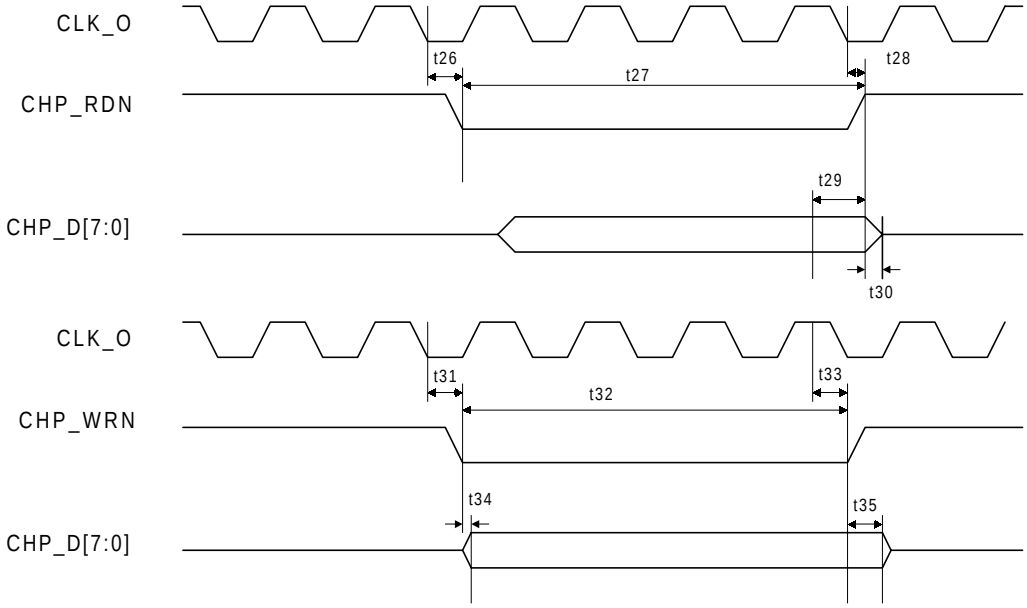




Reference	Parameter	5 Volts		3 Volts		Units
		Min	Max	Min	Max	
t18	CHS_I_STRB (CHS_O_STRB) hold (high to invalid)	5		5		ns
t19	CHS_I_STRB (CHS_O_STRB) Delay (high to invalid)		35		40	ns
t20	CHS_DI Setup (valid to high)	5		4		ns
t21	CHS_DI hold (high to invalid)	4		5		ns
t22	CHS_IBF or CHS_OBE Delay (high to high)		35		40	ns
t23	Enable CHS_DO Delay (low to active)		35		40	ns
t24	CHS_DO Delay (high to valid)		35		40	ns
t25	CHS_DO Hold (high to invalid)	5		5		ns

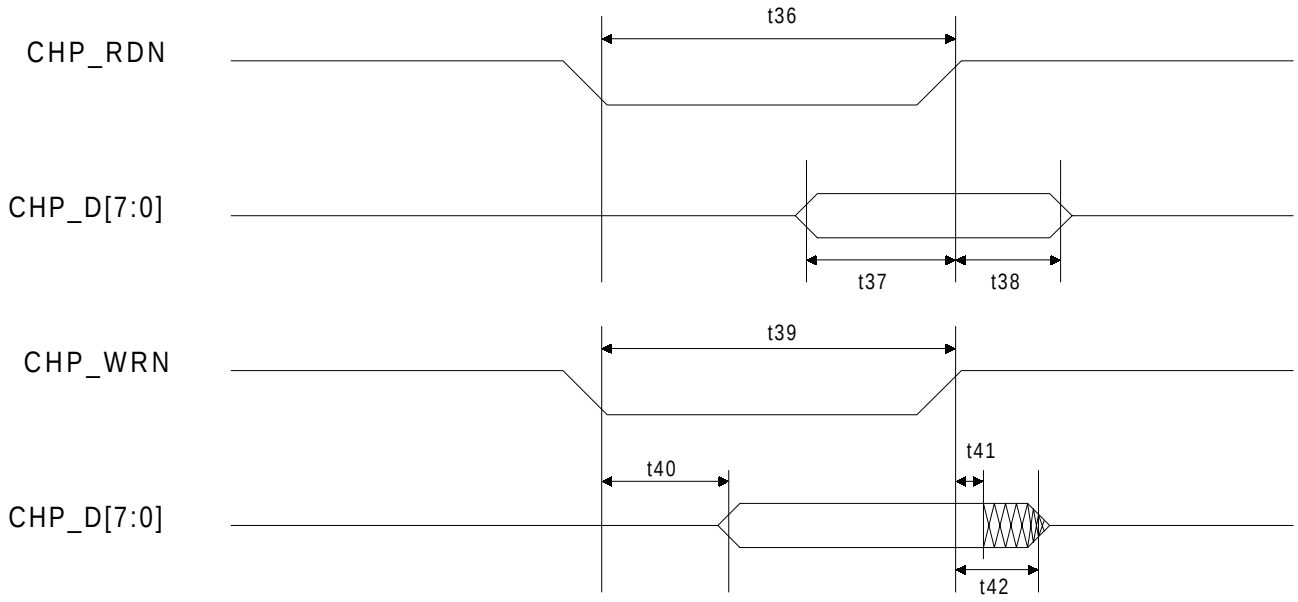
1.5.3 Channel Parallel Port

Timing Characteristics for Channel Parallel Port Operation in Active Packetized Mode



Reference	Parameter	5 Volts		3 Volts		Units
		Min	Max	Min	Max	
t26	CLK_O Low to CHP_RDN Assertion (Low to Low)		12		16	ns
t27	CHP_RDN Width (Low to High)	4T-4		4T-4		ns
t28	CLK_O Low to CHP_RDN Negation (Low to High)		10		18	ns
t29	CHP_D[7:0] Setup Time (valid to high)	8		8		ns
t30	CHP_D[7:0] Hold Time (high to invalid)	0		0		ns
t31	CLK_O Low to CHP_WRN Assertion (Low to Low)		12		16	ns
t32	CHP_WRN Width (low to low)	4T-4		4T-4		ns
t33	CLK_O Low to CHP_WRN Negation (Low to High)		10		18	ns
t34	CHP_WRN Low to CHP_D Valid (low to valid)		12		14	ns
t35	CHP_D Hold (high to invalid)	T/2 - 8		T/2 - 10		ns

Timing Characteristics for Channel Parallel Port Operation in Passive Packetized Mode



Reference	Parameter	5 Volts		3 Volts		Units
		Min	Max	Min	Max	
t36	CHP_RDN Pulse Width (Low to High)	T		T		ns
t37	CHP_D[7:0] Setup Time (valid to high)	8		8		ns
t38	CHP_D[7:0] Hold Time (high to invalid))	0		0		ns
t39	CHP_WRN Pulse Width (Low to High)	T		T		ns
t40	CHP_WRN Low to CHP_D Valid		28		34	ns
t41	CHP_D[7:0] Hold Time (high to invalid))	6		6		ns
t42	CHP_WRN High to CHP_D 3-state (Low to High)		20		37	ns

1.6 A/D-D/A Information

The following sections are provided to help the reader connect the AMBE-1000™ to the PCM A/D-D/As listed in this manual. For further information on the referenced A/D-D/A chips, please see the appropriate manufacturers data book or call DVSI for more information.

1.6.1 AT&T CSP1027

Reference:
(2) *AT&T Wireless Products Data Book,* AT&T Microelectronics September 1995, pages 11-1 through 11-60

The AMBE-1000™ has been pre-configured to work with the CSP1027 when the CSP1027 is placed into active mode. To place the CSP1027 into active mode, connect SMODE0 to V_{DD} and connect SMODE1 and SMODE2 to ground. This is shown in Figure App1.4.1-1.

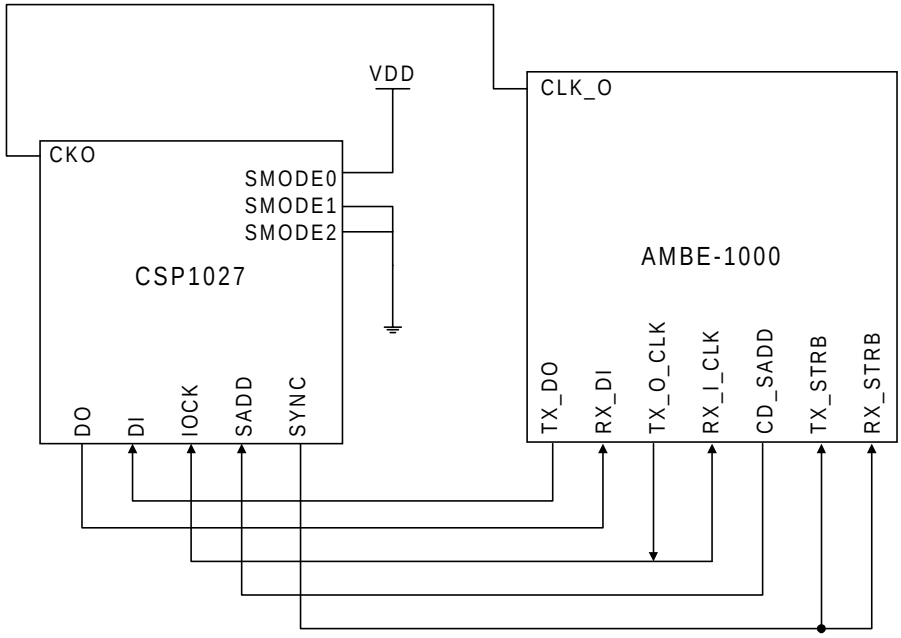


Figure App1.4.1-1 Connection diagram of the AMBE-1000™ and AT&T's CSP1027

In this configuration the CSP1027 supplies the input/output load, or SYNC, and the AMBE-1000™ will supply the serial clock. When the AMBE-1000™ is configured for packetized mode, after power-up or reset the AMBE-1000™ can send out a packet to the A/D-D/A that will contain information for the control registers. The control register information must be passed to the AMBE-1000™ in the first packet of data. This packet must be of ID type 0x03 (Speech Configuration with Control Data; see section 3.1.1.2) and the control data information will contain the CIOC information for the A/D-D/A plus some other information needed for the AMBE-1000™. Table App1.4.1-1 shows two different settings for the control data part of the packet. DVSI recommends settings shown in Table App1.4.1-1 for the CIOC registers. Please note that if the AMBE-1000™ is set up

for parallel packetized mode, the words shown in Table App1.4.1-1 must be sent to the AMBE-1000™ in bytes, high byte first.

Parameter	Microphone input	Auxiliary input		
Header	0x13ec	0x13ec		
ID / Flags	0x0300	0x0300		
Control 1 (AMBE-1000™ word 0)	0x03c8	0x03c8	Control Data	Values for CIOC registers can be different.
Control 2 (AMBE-1000™ word 1) [Enable AMBE-1000™ features]	0x0000	0x0000	Flags	These values are sent when the appropriate codec configuration is selected
Control 3 (AMBE-1000™ word 2) [One minus the # of words sent to the A/D-D/After this point]	0xfffd	0xfffd	Control Data 1 - 4 = -3	
Control 4 (CIOC0)	0x1ec0	0x1ea0	A/D-D/A Reg.	
Control 5 (CIOC1)	0x4020	0x4020	A/D-D/A Reg.	
Control 6 (CIOC2)	0x800f	0x800f	A/D-D/A Reg.	
Control 7 (CIOC3)	0xd000	0xd000	A/D-D/A Reg.	
Control 8	0x0000	0x0000	|	
Control 9	0x0000	0x0000	|	
Control 10	0x0000	0x0000	|	
Control 11	0x0000	0x0000	|	
Control 12	0x0000	0x0000	|	
Control 13	0x0000	0x0000	|	
Control 14	0x0000	0x0000	|	
Control 15	0x0000	0x0000	↓	

Table App 1.4.1-1 Example control packets for the AMBE-1000™ that will contain the AT&T's CSP1027 control registers

Some Helpful Notes

The AMBE-1000™'s CD_SADD signal is a serial address line that is used on the CSP1027. This signal determines whether the data coming from the AMBE-1000™'s TX_DO signal is **data OR control information**. When data is sent to the CSP1027, the CD_SADD signal will be a logical one

with every bit sent. If control information is being sent to the CSP1027, the first bit of each control **byte** sent will be a logical zero. Figure App1.4.1-2 shows and example of data and control information relative to the CD_SADD signal. See the AT&T data book for a description of the CSP1027's control words.

```
CD_SADD =       0 1 1 1 1 1 1 1 0 1 1 1 1 1 1 1
Control data =  0 0 0 1 1 1 1 0 1 1 0 0 0 0 0 0

CD_SADD =       1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
data  =         0 1 0 0 0 1 1 0 1 0 1 0 1 0 1 0
```

Figure App1.4.1-1 Example of CD_SADD Signal with Control Information and Data Information

1.6.2 Motorola MC145480

Reference:
(3) *Motorola Communications Device Data*, DL136/D REV 4 Q1/96, pages 2-1067 through 2-1088

This A/D-D/A can be used in either A-law or μ-Law mode. Figure App1.4.2-1 shows the recommended circuit that should be used to generate the clock and strobe signal to the AMBE-1000™ and the MC145480. In conjunction with this circuit, the AMBE-1000™ must be set to the correct A/D-D/A setting to interface correctly with the MC145480. Table 2.3-1 for the correct pin setting.

For more information about this Motorola A/D-D/A chip, see reference (3). If there are any questions about the drawing shown in figure App1.4.2-1, please contact DVSI.

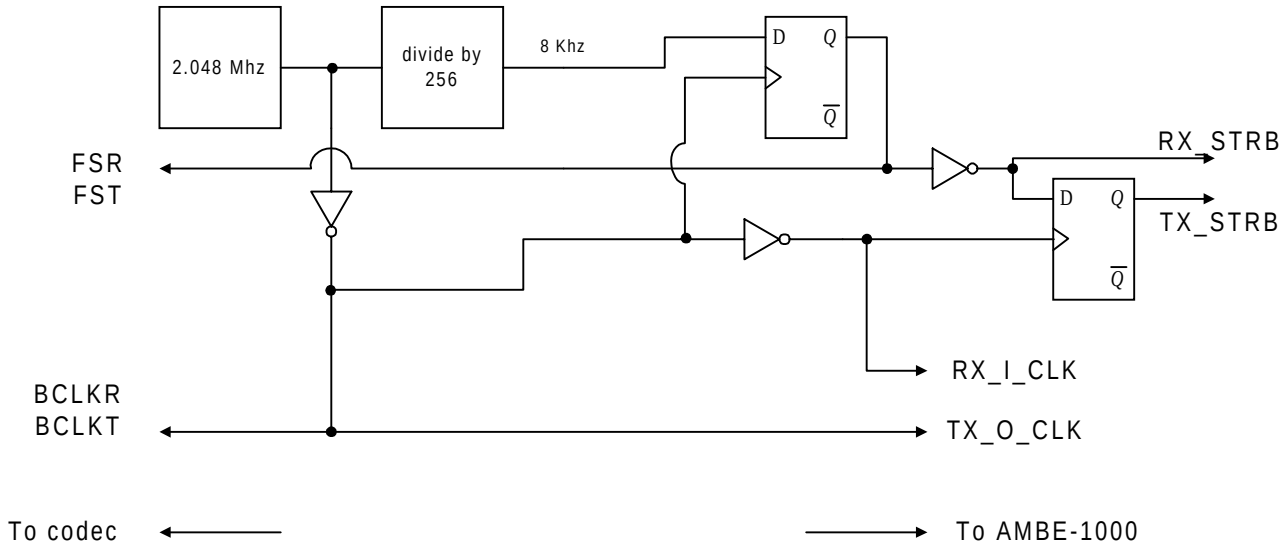


Figure App1.4.2-1 Circuit diagram to connect the AMBE-1000™ to the MC145480

1.6.3 TI TLC32046

Reference:
(4) *Texas Instruments Data Acquisition Circuits Data Book*, 1995, pages 7-3 through 7-57

The recommended interface circuitry to the AMBE-1000™ from the TLC32046 is shown in figure App1.4.3-1. The AMBE-1000™ A/D-D/A pin setting is shown in Table 2.3-1.

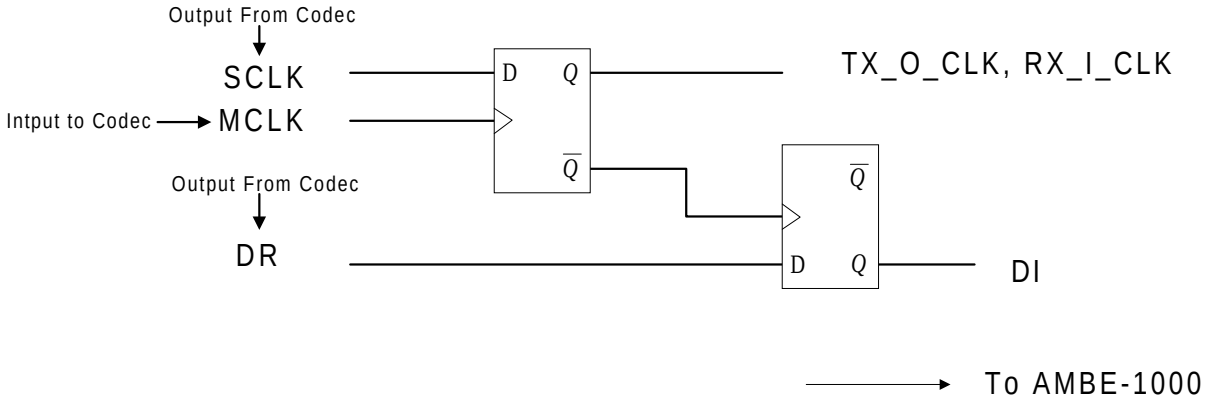


Figure App1.4.3-1 Circuit diagram to connect the AMBE-1000™ to the TLC32046

The TLC32046 is a programmable A/D-D/A and the first packet that must be sent to the AMBE-1000 is a A/D-D/A control packet that will program the TLC32046. Table App1.4.3-1 shows the correct packet to send to the AMBE-1000™.

Parameter	Frame Packet
Header	0x13ec
ID / Flags	0x0300
Control 1 (AMBE-1000™ word 0)	0x03c8
Control 2 (AMBE-1000™ word 1) [Enable AMBE-1000™ features]	0x0200
Control 3 (AMBE-1000™ word 2) [One minus the # of words sent to the A/D-D/After this point]	0xffff
Control 4 TI control setting	0x0003
Control 5 TI control register setting	0x02a7
Control 6	0x0000
Control 7	0x0000
Control 8	0x0000
Control 9	0x0000
Control 10	0x0000
Control 11	0x0000
Control 12	0x0000
Control 13	0x0000
Control 14	0x0000
Control 15	0x0000

Values for CIOC registers can be different.

These values are sent when the appropriate codec configuration is selected

Table App 1.4.3-1 Example control packet for the AMBE-1000™, to set TI's control registers

1.7 Special Handling Instructions

CAUTION

The foundry recommends certain handling precautions when the AMBE-1000™s are removed from its moisture sealed package. DVSI may re-package the AMBE-1000™ when small volumes of devices and/or odd lot sizes are requested. The following are the foundry's suggested handling instructions.

1. Shelf life in moisture controlled package: 12 months at <40°C and < 90% RH.
2. After moisture controlled package is opened, devices that will be subjected to infrared reflow, vapor-phase reflow, or equivalent processing (peak package body temperature. 220°C) must be:
   a) Mounted within 168 hours at factory conditions of $\leq$30°C / < 60% RH, or
   b) Stored at $\leq$ 20% RH.
3. Devices require baking, before mounting, if:
   a) Humidity indicator card > 20 % when read at 23°C $\pm$ 5°C, or
   b) 2a or 2b are not met.
   c) Devices were not shipped in a package designated as "moisture controlled."
4. If baking is required, devices may be baked for
   a) 192 hours at 40°C $\pm$ 5°C / -0°C and < 5% RH for low-temperature device containers, or
   b) 24 hours at 125°C $\pm$ 5°C for high-temperature device containers