

Compact Ovenized Crystal Oscillators with Internal Synchronization to Standard Frequency Transmitters

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1. Introduction

Ovenized crystal oscillators (OCXO) show a very low phase noise and excellent short-term stability. The long-term behaviour is determined mainly by the aging of the crystal oscillator, for AT-cut and SC-cut that is between 10^{-8} and 10^{-6} per year. Most application therefore require to re-adjust the oscillator after a certain time to compensate for the aging.

Many OCXOs produced today are used in base stations and other remote locations where the readjustment is extremely difficult. Synchronization to a standard frequency transmission of one of the VLF transmitters is favourable and allows to achieve a long-term stability of 10^{-9} , while the short-term stability still is determined by the OCXO.

This table presents a solution in which the complete OCXO plus the VLF receiver and the frequency synchronization circuit are included in a very compact enclosure of the size $67 \times 60 \times 40 \text{ mm}^3$ (2,6" x 2,4" x 1,6"). The whole unit is not larger than a conventional OCXO. For interference-free reception an external antenna can be connected to a coaxial cable.

2. Synchronization requirements

VLF transmitters for standard frequencies are used throughout the world. In Germany the transmitter DCF-77 at 77,5 KHz, located near Frankfurt/Main, Germany, is the legal distributor of time and frequency. Its output frequency is based on three high accuracy primary cesium standards of the German standards authority PTB (German equivalent of NIST). Similar transmitters in Central Europe are HBG (Switzerland) at 75 KHz, OMA (Czechia) at 50 KHz, MSF and GBR (UK) at 60 KHz resp. 16 KHz. In the US OMEGA and LORAN C transmitters can be used as a reference.

The frequency accuracy which can be recovered by a VLF receiver is degraded by variations in the propagation conditions (delay, reflexions, etc.) and also by a pseudo-random phase keying of the DCF-77 carrier which was introduced in 1983. Therefore, the inherent stability of the Cs sources can only be approached for averaging times longer than one day. Figure 1 shows the frequency stability vs. averaging time (Allan-Variance) for different sources. The dotted line marked 'DCF' is the useable accuracy of a DCF signal received approximately 300 km from the transmitter. The shaded area marked 'Q' indicates the typical range for crystal oscillators.

Synchronization of an OCXO to a VLF reference transmitter therefore imposes the following requirements:

- the good short-term stability of the OCXO shall not be degraded by the synchronization
- very short distortion and interferences of the reception is caused by man made noise, ignitions, thunderstorms, etc. must be isolated from the OCXO
- at interruptions of the transmission or other loss of synchronization the OCXO frequency shall not float
- the stabilization characteristic of the OCXO after power-on shall not be degraded by the required synchronization

The aim of the presented development was:

- the whole oscillator including the VLF receiver and the synchronization has to be included in a conventional OCXO
- the current consumption shall be approximately the same as for already existing OCXOs
- the efforts for tuning and adjustment of the whole unit should be minimized.

All these requirements could be fulfilled by the presented solution

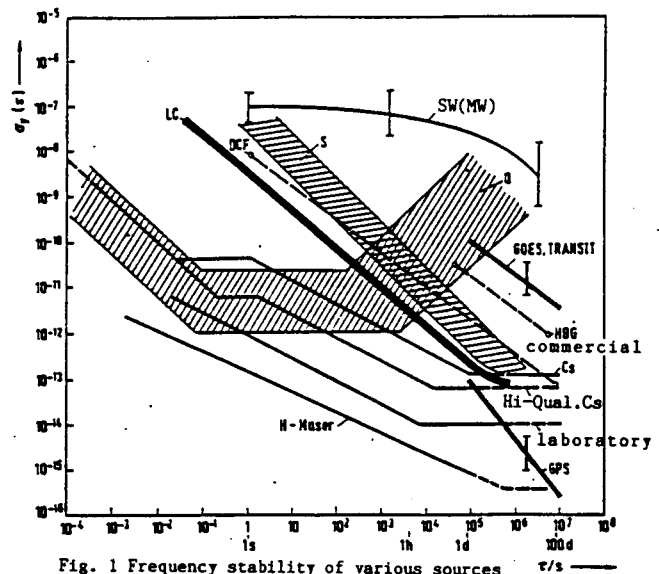


Fig. 1 Frequency stability of various sources τ/s

3. Description of the device

Because of the small available space, concept using complicated synthesizers and multiple PLL loops could not be used. The required high time constants in excess of one day in connection with the fast warm-up characteristic required are not easily realizable with conventional PLL circuits. Because of space restrictions and to avoid adjustment the whole receiver circuit in the unit does not use any inductors. The method described below does not deteriorate the characteristics of the precision OCXO and nevertheless is realized with relatively low parts count. The aim of the method was to reach a frequency stability in the order of $\pm 1 \cdot 10^{-9}$ by a suitable frequency locking principle, not a phase locking loop. Thus, the OCXO is not locked strictly to the phase of the VLF standard frequency transmitter which is the cause of the complexity of usually applied PLL circuits. The frequency control loop is realized by a low-cost micro-controller with peripheral circuits (counter, D/A converter etc.). The main design work therefore is concentrated in the software of the system, while hardware requirements are reduced drastically. Figures 2 and 3 shows the working principle of the circuit. Four functional blocks are shown:

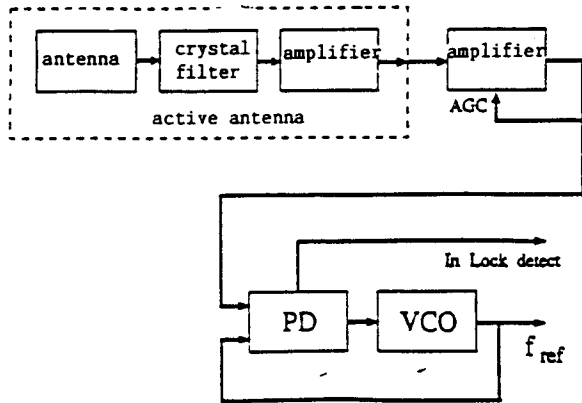


Fig. 2 Building blocks of the frequency synthesis

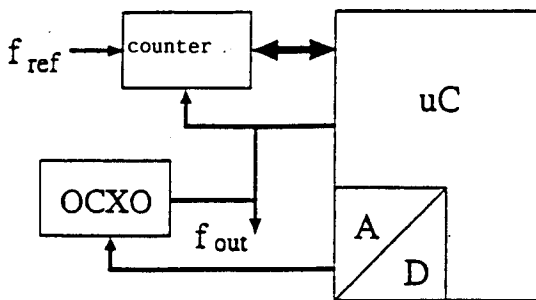


Fig. 3 Building blocks of the digital part

- receiver
- tracking oscillator (used as tracking filter)
- precision OCXO
- micro-controller

The receiver consists of an active antenna, whose DC supply is delivered through the coaxial connection to the OCXO unit. The transmitted standard frequency is picked up by a tuned ferrite antenna. It is combined with a single-pole crystal filter which filters the incoming signal with a bandwidth of approximately 2 to 3 Hz. This small bandwidth already suppresses a large amount of the amplitude modulation of the transmitter (time and date coding). The circuit is given in figure 4. The capacitor C3 in the opposite lattice branch the filter can be adjusted either to a symmetrical response or to a response with a finite attenuation pole at a given interference frequency. Because of the good filtering of a received signal direct at the front end of the receiver, disturbing and interfering signals and frequencies in the vicinity are effectively filtered out, so that they cannot cause any overdrive and limiting actions of the subsequent stages or even blocking of them. The inclusion of the filter in the antenna preamplifier leads to a significant space reduction for the receiver itself. The following preamplifier has a high input impedance and a gain of approximately 6. An emitter follower matches the amplifier to the cable impedance of 50 Ω . The total current consumption of the preamplifier is 1.7 mA. For a sufficient reception quality the antenna unit should be mounted away from the system at a high position. The ferrite stick should be oriented for maximum sensitivity in the direction of the transmitter.

The signal from the antenna preamplifier goes into the receiver which is included in the OCXO unit. The input impedance of T3 is matched to 50 Ω . The voltage gain is approx. 80. The following transistor T4 couples the amplified AC-voltage into IC1 of a low impedance. IC1 contains 2 amplifiers with controllable gain and an AGC circuit which maintains the output signal at pin 8 at a constant level of 90 mV_{rms}. The time constant of the AGC is such that the residual amplitude modulation of the DCF-77 signal is suppressed completely. At the collector of T5

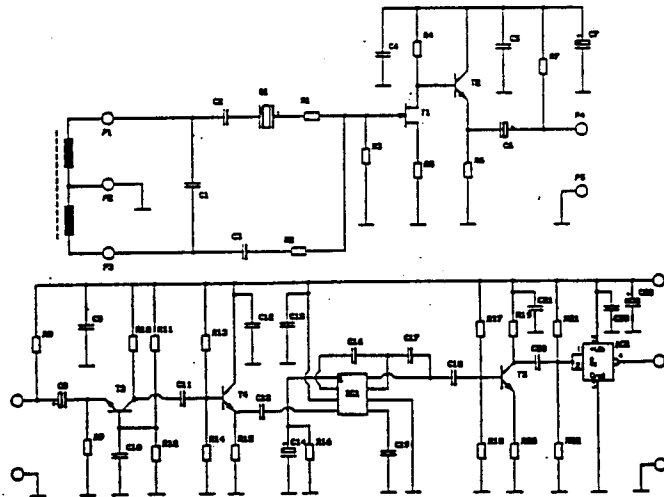


Fig. 4 Circuit diagram of the receiver

we get a sinusoidal AC-voltage which is shaped into a clean rectangular signal used for the processing with the following digital components by IC2. The maximum overall gain of the receiver circuit is 132 dB. That is sufficient for application throughout Germany and in most parts of Central Europe. The dynamic range of the AGC circuits is approx. 55 dB. In areas with extremely high field strength, e. g. close to the transmitter, the signal is already limited in the amplifier stages in front of the AGC control. This, however, has no negative influence on the subsequent stages because the above-mentioned modulation of the DCF-77 signal is not desired anyhow. In those cases the AGC control is not effective.

The squared signal at the output of the receiver has a very poor short-term stability and high jitter. This is improved by the following tracking filter, which can be operated with very narrow bandwidth by a crystal stable oscillator. With a loop time-constant of 3 ... 5 seconds the phase jitter of the signal can be improved significantly. Because of the fact that PLL circuits work like ideal bandpass filters beyond their open loop bandwidth, interferences with very short time constants are suppressed effectively by the circuit. The output of this VCXO delivers a square wave signal which represents the received carrier with moderate short-term stability. In case of carrier loss or of longer lasting interferences an integrated in lock detector delivers an "out-of-lock signal" to the micro-controller. Thus, erroneous synchronizations are avoided effectively. For short-term carrier interruptions the PLL is able to deliver a carrier signal for some time with approximately correct phase. Thus, short interferences by thunderstorms, ignitions etc. have no influence on the function of the circuit. The PLL circuit consists of a standard CMOS IC 4046, from which only the phase detector and the lock detector are used. Despite the only partial use of this IC this solution was found to be the optimum between current consumption and space requirement.

The cleaned output signal of the described circuit is now fed into the digital portion of the unit (figure 5). This part performs the synchronization of the OCXO to the received standard frequency.

The received and processed carrier signal goes to a flip-flop (IC1) which can reset the counter (IC2) through the micro-controller. The beginning of the count is synchronized with the falling edge of the standard frequency signal. At the same time the prescaler, which is part of the IC 1, is activated. The micro-controller divides the input frequency further down by software. By this, very long time constants can be realized. The output frequency of the OCXO is continuously measured in IC2. Because of the high frequency stability of the OCXO (in short terms) it is sufficient that the counter of IC 2 is read only once a second. As long as the frequency of the OCXO does not move more than 64 Hz (at a nominal frequency of 10 MHz), no information is lost by a probable counter overflow, which occurs every 12,8 μ sec. This condition is fulfilled for all OCXOs without problems.

The counter is read out by the shift register IC3. The inputs of the shift register are latched, so that the processor has sufficient time to read the counter serially. IC4 computes the

required pulling voltage for the OCXO by a numerical method. This voltage is output serially via a 12 bit D/A-converter which was extended to 14 bit resolution by additional resistors. For a pulling range of ± 2 ppm (10^{-6}) this leads to a resolution of 0,25 ppb (10^{-9}). The clock of the micro-controller is derived from the output frequency in IC2. Additional clock generators are not necessary. The whole microprocessor control circuit is located on a small double-sided SMT pc-board which is mounted vertically on the OCXO board.

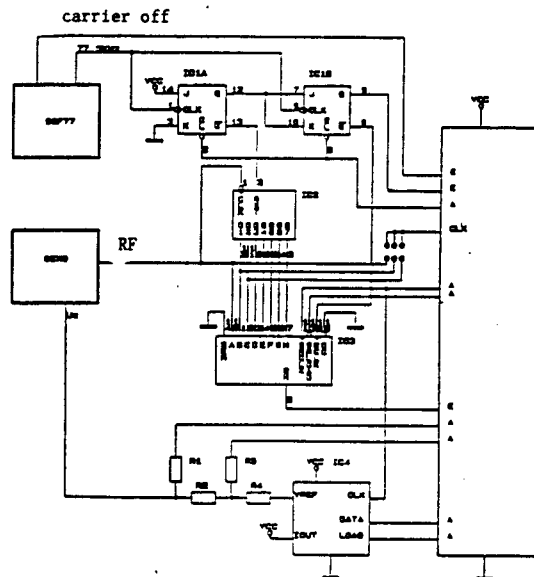


Fig. 5 Digital synchronization unit

4. Software

The flow chart of the software routines are given in figure 6. After the switch-on of the system, a pulling voltage for the OCXO is generated by the use of a parameter stored internally in the EEPROM of the micro-controller. This parameter is individually derived from the measurement during production of the unit. Therefore, the OCXO skips nearly immediately to nominal frequency even at the first operation. The value of the pulling voltage is continuously renewed, so that the output frequency is also recovered very fast after a power-down. Also after loss of the standard frequency carrier the stored value is used. After a suitable warm-up time, depending on the used oscillator type (5 to 15 minutes), the controller starts with the synchronization. From the standard frequency signal interrupts are derived which decrements a software based counter. Each second the counter overflows, which is used to read out the counter of IC2. My means of a digital controlled algorithm the correction values for the D/A-converter are computed from the measured values. The frequency error of the OCXO therefore is well below 1 ppb as long as the standard frequency carrier can be received. If no carrier is present the last correction value in the EEPROM is frozen. This means that the aging of the oscillator follows the regular aging curve of the free running OCXO for this short period.

Figure 7 shows a typical example of a practically measured "aging curve" of a OCXO unit synchronized to DCF-77 by the described method.

5. Summary

The paper describes a compact ovenized crystal oscillator which is internally synchronized to a standard frequency transmitter in the VLF range. The received signal is cleaned up by analogue and digital circuitry. The synchronization is realized by software which is run in a micro-controller. All components, receiver, clean-up circuitry micro-controller, OCXO (except the antenna) are included in a conventional OCXO enclosure. The current consumption of the synchronization unit is only a small fraction of the overall current consumption of the OCXO circuit itself.

The method allows the aging of an OCXO to be kept below $1 \cdot 10^{-9}$ for the whole life time of the OCXO. The sensitivity to external interferences, carrier loss, etc. are minimized.

6. References

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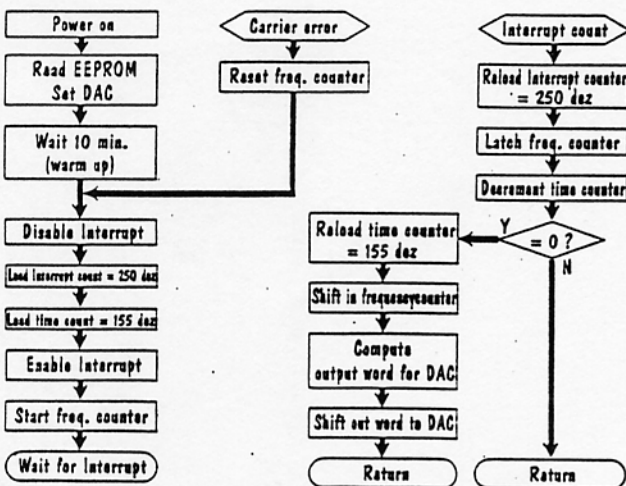


Fig. 6 Flow chart of the synchronization algorithm

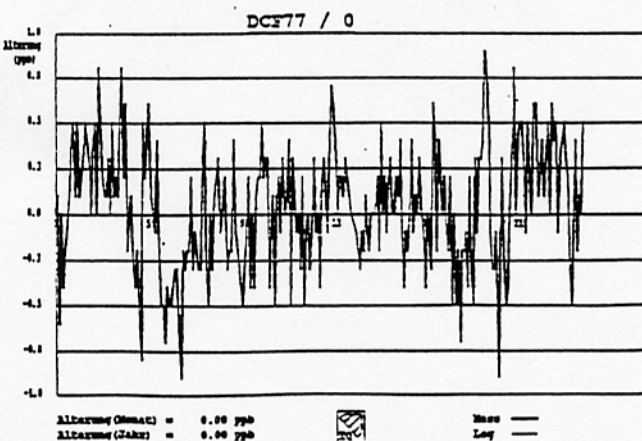


Fig. 7 Typical aging results